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A Motor friendly Quasi-resonant DC-link Inverter

genehmigte
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von
Jayalakshmi Kedarisetti, M.Tech.
aus East Godavari/Indien

Referent:	Prof. Dr.-Ing. Peter Mutschler
Korreferent:	Prof. Dr.-Ing. Axel Mertens
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Jayalakshmi Kedarisetti, M.Tech.
Geboren am 04. März 1982 in East Godavari, Indien

Referent:	Prof. Dr.-Ing. Peter Mutschler
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Abstract

Feeding electrical motors by long cables using PWM inverters has become lately problematic due to developments in semiconductor technology. Most used in converters, insulated gate bipolar transistors IGBTs switch voltages with high gradients, about 10kV/µs. On one hand, faster switching transients lead to the reduction of switching losses and therefore, permissible higher switching frequencies, reduction of harmonics and audible noise at motors. On the other hand, bigger voltage gradients combined with long feeders lead to high frequency parasitic effects, like overvoltage at motor terminals leading to insulation stress, high common mode (CM) ground current, bearing currents, etc. Up-to-date several approaches have been made to overcome these problems. The most common solution is the use of filter between inverter and motor. But it increases the size, weight and cost of the inverter. This thesis investigates an alternative solution to high frequency parasitic effects in electrical drives with long cables.

Quasi-resonant DC-link (QRDCL) converter topologies can be used in electric drives with long cables to reduce the parasitic effects. In a QRDCL converter, the slope of the output voltage can be reduced by means of resonant operation. A resonant cycle can be initiated at any time using auxiliary switches (therefore, the name quasi-resonant) making it suitable for PWM operation. A resonant cycle produces a zero voltage interval, and it can be used as a zero vector state in a PWM modulation. Further, by separating the DC-link during resonant operation (used as a zero voltage vector) the common mode voltage is reduced from its peak values ($\pm V_{dc}/2$) to zero, determining the important reduction of bearing currents.

The thesis concentrates on motor-friendly and high efficient design of a QRDCL converter and its control implementation on FPGA. A 30m long cable connected between inverter and motor produces the voltage reflections and causes high frequency noises in motor. For allowed 20% of overvoltage at motor terminals, a maximum slope gradient of 600V/µs at inverter output is needed. The slope of the quasi-resonant inverter output voltage depends upon its three passive elements and load current. The design complexity increases with more design constraints like reduced voltage stress on switching devices. In this thesis, the selection of passive elements is discussed in detail.

The trip currents selection in a resonant cycle ensures the completion of a resonant cycle. But very high trip currents produce losses and reduce the overall efficiency of an inverter. The complexity is increased with three passive elements and higher number of modes in a given resonant cycle. For given resonant elements, the optimal calculation trip currents based on the load currents is discussed in this thesis.

For control of a resonant circuit, a fast controller like FPGA is needed. For the induction motor control, same FPGA can be used. It reduces the total hardware count and provides a low-cost solution. The parallel processing FPGA is advantageous because of its high speed but imposes an additional challenge in programming. Moreover, it is a fixed-point FPGA. The implementation of field oriented control and control of a quasi-resonant inverter are discussed in this thesis.

A motor friendly quasi-resonant dc link inverter is being designed and experimentally tested. The soft switching inverter is then compared with the conventional hard switched voltage source inverter together with filter under identical load conditions. At low modulation index, the resonant cycles are longer due to long zero voltage vector. During a zero voltage vector, resonant inductor current free wheels through an auxiliary diode and inverter switches. Higher the freewheeling time, more losses will be produced.

This effect is observed in efficiency measurements. So a lossless variable zero voltage duration is necessary for high efficiency of the QRDCL inverter.

At the end, a motor friendly quasi-resonant DC-link inverter with loss less variable zero voltage is proposed. The performance of this QRDCL inverter is verified through the simulations.

Kurzfassung

Die Versorgung elektrischer Motoren über lange Kabel und die Verwendung von Wechselrichtern ist heutzutage eine Problematik aufgrund der Entwicklung in der Halbleitertechnologie. Die meisten, der in heutigen Umrichtern verwendeten Insulated Gate Biolar Transistoren (IGBT), schalten Spannungen mit hohen Spannungssteilheiten um ca. 10kV/µs. Auf der einen Seite führen schnellere Schalt-Transienten zur Verringerung von Schaltverlusten und daher zu höher zulässigen Schaltfrequenzen, zur Reduzierung von Oberschwingungen und zu hörbaren Geräuschen in den Motoren. Auf der anderen Seite führen größere Spannungsgradienten in Kombination mit langen Kabeln zu hochfrequenten parasitären Effekten wie Überspannung an den Motorklemmen und somit zu Isolationsproblemen, zu hohen Gleichtaktströmen, zu Lagerströmen usw. Es wurden verschiedene Ansätze unternommen um diese Probleme zu überwinden. Die häufigste Lösung ist der Einsatz eines Filters zwischen Wechselrichter und Motor. Aber es erhöht die Größe, das Gewicht und die Kosten des Wechselrichters. Diese Arbeit untersucht eine alternative Lösung um die hochfrequenten parasitären Effekte in elektrischen Antrieben mit langen Kabeln zu mindern.

Quasi-resonanter DC-link (QRDCL) Umrichter können bei elektrischen Antrieben mit langen Kabeln verwendet werden, um die parasitären Effekte zu reduzieren. In einem QRDCL-Umrichter die Steigung der Ausgangsspannung kann durch resonanten Betrieb reduziert werden. Ein Resonanzzyklus kann jederzeit unter Verwendung eines Hilfsschalters eingeleitet werden (daher der Name quasi-resonant) und eignet sich deshalb für den PWM-Betrieb. Ein Resonanzzyklus erzeugt ein Nullspannungsintervall und kann somit als Nullvektor in einer PWM-Modulation verwendet werden. Durch die Trennung des DC-Links im resonanten Betrieb (verwendet als Null-Vektor) wird die Gleichtaktspannung von ihren Höchstwerten ($\pm V_{dc}/2$) auf Null reduziert und führt somit zur wichtigen Verringerung der Lagerströmen.

Diese Arbeit beschäftigt sich mit einem motorfreundlichen und hocheffizienten Design eines QRDCL-Wechselrichters und seiner Kontrollimplementierung auf Field Programable Gate Arrays (FPGA`s). Ein 30m langes Kabel zwischen dem Umrichter und dem Motor generiert Spannungsreflexionen und verursacht somit hohe Frequenzen im Motor. Für eine maximal zulässige 20% Überspannung an den Motorklemmen wird eine maximale Spannungssteilheit von 600V/µs am Wechselrichterausgang benötigt. Die Spannungssteilheit der quasi-resonanten Wechselrichterausgangsspannung hängt von den drei passiven Bauelementen und dem Laststrom ab. Die Komplexität des Designs steigt mit der Designforderung nach reduzierter Spannungsbelastung der Schaltgeräten. In dieser Arbeit wird die Auswahl der passiven Elementen im Detail besprochen.

Die Auslösestromauswahl garantiert die Fertigstellung eines Resonanzzyklusses. Aber sehr hohe Auslösestrome erzeugen Verluste und verringern den Gesamtwirkungsgrad eines Wechselrichters. Die Komplexität erhöht sich um drei passive Elemente und wegen der höheren Anzahl von Arten in einem gegebenen Resonzzyklus. Für vorgegebene Resonanzelemente wird in dieser Arbeit die optimale Berechnung der Auslöseströmen auf der Basis der Lastströme diskutiert.

Für die Steuerung eines Resonanzschalters wird eine schnelle Steuerung durch z.B. FPGA benötigt. Für die Steuerung von Asynchronmotoren kann die gleiche FPGA verwendet werden. Damit es reduziert sich die Hardware und eine kostengünstige Lösung ist möglich. Die parallelverarbeitende FPGA ist wegen ihrer hohen Geschwindigkeit von Vorteil, ist aber eine zusätzliche Herausforderung bei der Programmierung. Darüber hinaus besitzt die FPGA eine Festkommaarithmetik. Die Umsetzung der feldorientierten

Regelung und Steuerung eines quasi-resonanten Wechselrichters werden in dieser Arbeit diskutiert.

Ein motorfreundlicher QRDCL-Wechselrichter wurde entworfen und experimentell getestet. Der QRDCL-Wechselrichter wurde mit konventionellen hartgeschalteten Wechselrichtern und den Ausgangsfiltern unter identischen Lastbedingungen verglichen. Bei niedrigem Modulationsindex werden die Resonanzzyklen wegen des langen Nullspannungszeigers länger. Während der Zeit eines Nullspannungszeigers fließt der Resonanzstrom durch die Resonanzdiode und die Wechselrichterschaltungen. Je höher die Freilaufzeit desto höher werden die Verluste. Dieser Effekt ist in Effizienzmessungen beobachtet worden. Eine verlustfreie variable Nullspannungszeitdauer ist für einen hohen Wirkungsgrad des QRDCL-Wechselrichters erforderlich.

Am Ende wird ein motorfreundlicher QRDCL-Wechselrichter mit verlustfreier variabler Nullspannung vorgeschlagen. Die Funktionalität dieses QRDCL-Wechselrichters wurde durch Simulationen belegt.

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List of Symbols and Abbreviations

AC	: Alternating Current
ADC	: Analog to Digital Converter
AHDL	: Altera Hardware Description Language
AMI	: Antrieb Module Interface
BJT	: Bipolar Junction Transistor
C	: Snubber Capacitor
C_{add}	: Added capacitance for voltage balancing
C_{eq1}, C_{eq2}	: Equivalent stray capacitances across MOSFET drain to source
CM	: Common mode
CMV	: Common mode voltage
CPLD	: Complex programmable logic device
C_r	: Resonant Capacitor
CSI	: Current Source Inverter
DAC	: Digital to Analog Converter
DC	: Direct Current
DCG	: DC generator
DDR SDRAM	: Double data rate synchronous dynamic random access memory
DFG	: Deutsche Forschungsgemeinschaft
D_r & D_{r1}	: Resonant circuit diodes
EMC	: Electromagnetic Compatibility
EMI	: Electromagnetic Interferences
FPGA	: Field Programmable Gate Array
GTO	: Gate Turn-off Thyristor
HF	: High Frequency
IFOC	: Indirect field oriented control
IGBT	: Insulated Gate Bipolar Transistor
i_L	: Resonant inductor current
IM	: Induction motor
I_O, I_{OX}	: Present and next inverter bridge input currents
I_P, I_{Tp1}, I_{Tp2}	: Trip currents
L_r	: Resonant Inductor
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
PCB	: Printed circuit board
PI	: Proportional integral
PWM	: Pulse width modulation
RB	: Reverse blocking
QRDCL	: Quasi resonant DC-link
QRDCLI	: Quasi resonant DC-link inverter
SCR	: Silicon Controlled Rectifier
S_{DC1}, S_{DC2}	: DC-link switches
SiC	: Silicon carbide
S_{INV}	: Equivalent switch for inverter bridge
S_r	: Resonant switch
SSRAM	: Synchronous Static Random Access Memory
SVPWM	: Space vector pulse width modulation
V_C	: Voltage across inverter bridge
V_{CM}	: Common mode voltage
V_{Cr}	: Resonant capacitor voltage
V_{DC}	: DC-link voltage
V_{DM}	: Differential mode voltage
VSI	: Voltage source inverter
ZCS	: Zero current switching
ZVP	: Zero voltage period
ZVS	: Zero voltage switching

1 Introduction

The chapter introduces electronically controlled speed adjustable drives. The effects of the fast switching semiconductors on motor connected through long cable are discussed. Then an introduction to the proposed method to mitigate the high frequency parasitic effects is provided. Finally, an overview of the thesis is given.

1.1 Back ground

Motor drives are used in wide varieties of industry and home applications. In the absence of any control, motor drives are fed directly from the mains supply and operate at a constant speed. For example, water pumps, fans, conveyers, etc. are usually connected directly to the main supply grid. In a pump driven at a constant speed, throttling valve controls the flow rate. These mechanisms waste lot of energy [1]. For the required air or water flow, the speed of the fans and pumps can be adjusted using adjustable speed drives. In earlier days, adjustable speed drives were realized by controlling gears, valves, hydraulic coupling, etc. The other method is combining several electrical machines. An example of this is a well-known Ward-Leonard drive. These methods are more complicated to implement in automated processes and have poor efficiency [1].

With the advent of power electronics, the control of adjustable speed drives is done by the power converters. Electrical drives with speed, torque and position control are increasingly being used in manufacturing, transportation systems, etc. [1]. The power converter unit gets its power from the single or three phase sinusoidal voltages of a constant amplitude and fixed frequency. The power converter unit converts the fixed input voltage to variable frequency and amplitude output, which is suited for the operating of the motor. Electrical drives operate either in an open loop or closed loop manner. In a closed loop manner, i.e. with feedback, a controller by comparing the input signals (like position, speed and torque) with the measured signals provides appropriate control signals. The power converter unit in response to the controller signals provides the right voltage and frequency to the motor. Systems with electronically controlled adjustable speed drives offer higher efficiency, simple construction, lower maintenance and easier control [1].

In all drives, where the speed and position are controlled, power electronic converter is used as an interface between input power and motor [2]. Historically, the silicon controlled rectifier (SCR) is the first power semiconductor device to be commercially available. Then the new devices available are gate turn-off thyristors (GTO), bipolar junction transistors (BJT), metal oxide semiconductor field effect transistors (MOSFET), insulated gate bipolar transistors (IGBT) and silicon carbide (SiC) devices, etc. These devices are fully controllable, fast turn-on and turn-off, low conduction losses and easier to control [4], [5]. These power devices are compared, and the applications are given in Table 1.1. All these devices along with SCRs are available for building power converters for feeding the AC motor drives [3], [6].

The power electronic converter topology and its control depend upon the type of the motor. In most of the industrial applications, induction motor drives with variable frequency power converters are used [1], [3]. The inverters used for the induction motor control are classified as pulse width modulated voltage source inverters (PWM-VSI) with a diode rectifier, square-wave voltage source inverters (square-wave VSI) with controlled rectifiers and current source inverters (CSI) [2]. For low power applications, PWM-VSI is generally used. Here, the input AC power is first rectified to the DC power using a diode rectifier. Then the DC power is converted to the motor input AC power using a power converter. This PWM inverter controls both the magnitude and frequency of the voltage input to the motor.

Table 1.1: Semiconductor devices

Device	Advantages & Disadvantages
SCR	▪ Gate turn-off is not possible ▪ Preferred for line and load commutated converters. ▪ Blocks both forward and reverse voltages ▪ Switching frequencies up to 1 kHz
GTO	▪ Gate drive is complicated ▪ Mostly used at high voltages and high power applications ▪ Blocks both forward and reverse voltages ▪ Switching frequencies up to 1 kHz
BJT	▪ High base currents are required. ▪ Low conduction losses ▪ Blocks only the forward voltage ▪ Switching frequencies below 10 kHz
MOSFET	▪ Easy to drive ▪ High conduction losses ▪ Blocks only the forward voltage ▪ High switching frequencies up to 100 kHz
IGBT	▪ Simple gate drive circuit ▪ Used for medium power to high power applications ▪ Blocks only the forward voltage (except RB-IGBTs) ▪ Switching speeds up to 20 kHz (hard switching)
SiC JFET	▪ Requires a negative voltage to turn-off → Complex drive circuit. ▪ Lower voltage drop ▪ High switching frequencies up to 500 kHz [7] ▪ Not commercially available (2011)

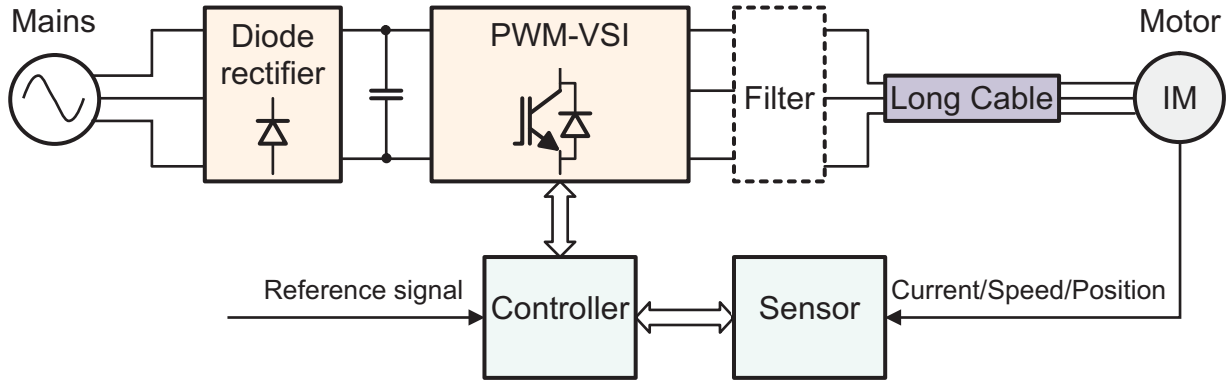


Figure 1.1 Block diagram of an electric drive system

If a long cable is necessary between the motor and voltage source inverter, a filter may be necessary to reduce high frequency problems. In this case, a high switching frequency in PWM converters reduces the size and the weight of passive components and hence reduces the cost as well as weight of the power converters. In hard-switched power converters switching losses limit the applicable switching frequency. Switching with large

dv/dt reduces the switching losses. For medium power applications, IGBTs are used for constructing PWM-VSI. The new generation IGBTs are having a rise time of 50 ns with voltage gradients between 5 to 10kV/μs. So the switching losses in the IGBTs are considerably reduced. On the other hand, bigger voltage gradients combined with long feeders lead to high frequency parasitic effects, like over voltages at motor terminals, high common mode ground current, bearing currents, etc. These effects are discussed in the following section.

The block diagram of a PWM-VSI fed induction motor drive is given in Figure 1.1. The induction motor may be driven with either a long cable or a short cable. When the application demands the motor to be located far away from the inverter, for example, in underground mining industry or petrochemical plants, the motor should be connected through a long cable. The application of VSI can generate over voltages at motor terminals. In such a case, the most common solution is the use of output filters between inverter and motor. The use of the filters again increases the cost and weight of the power converters.

1.2 HF parasitic effects in electrical drives with long cables

The effects of using fast switching semiconductors with long cables are reported in the literature [8], [9], [10] and [12]. Voltage reflections are produced due to the impedance mismatch between cable and motor. High *dv/dt* and a high common mode voltage produce bearing currents.

Voltage overshoots and voltage peaks: PWM waves traveling on a long cable between inverter and motor behave like traveling waves on a transmission line [8], [12]. They produce high frequency oscillations and over voltages at the motor terminals [8], [9]. The voltage at the motor terminals can be double of the DC-link voltage [12]. For certain PWM modes, these reflections can be tripe or more than that [10]. Voltage reflection is a function of *dv/dt*, motor cable characteristics and high frequency surge impedance of the motor [12], [17]. Various technical standards recommend limits for the admissible voltage peak at motor terminals and *dv/dt* for different motor types [14], [17]. The allowed voltage gradient *dv/dt* decreases with the increase in cable length. The safe repetitive transient withstand level is often termed as a voltage peak of 1000 V and voltage gradient 500 V/μs, at the motor [11], [14].

High frequency (HF) noise: The ringing voltage at the motor terminals, due to the high *dv/dt* and motor cable, causes high frequency noise [14]. HF noise is also caused by the CM voltage between phases and ground, and switching of the semiconductors [17]. The CM ground currents occur due to the capacitive coupling between cable and earth and between stator windings and frame. These currents flow from three phases to ground through distributed capacitances [18]. The CM ground currents cause EMI, interference with the ground fault protection systems, induction of high frequency circulating bearing currents, and rotor ground currents [20].

Bearing currents: The bearing currents due to the fast switching IGBTs are reported in [20]. The bearing currents depend upon the size of the motor, rate of the rise of the CM voltage and level of the CM voltage.

Capacitive bearing currents: The common mode voltage at the stator windings causes a voltage drop (V_b) across the bearing owing to the capacitive coupling between rotor and stator windings and between the rotor and the frame. The *dv/dt* over the bearing

causes along with the bearing capacitance small capacitive bearing currents. However, these currents are negligible and typically do not cause any bearing damage [15], [20].

Electrostatic discharge currents: When the bearing voltage (V_b) exceeds the threshold voltage, the lubrication film between balls and running surface discharges, causing electro static discharge currents. Larger duration and repetition of these voltages will lead to metallic wear and bearing break down. The resulting currents will be in the order of (0.5...3 A) and harmful, especially for small motors [20].

Circulating bearing currents: The high *dv/dt* at motor terminals along with the stator windings to frame capacitance cause an additional ground current. This ground current excites a magnetic flux in the shaft, and a voltage is induced along the shaft. If this shaft voltage is high enough to puncture the lubricant film of the bearings, it causes a circulating bearing current along the stator frame – non drive end – shaft – drive end [20]. These bearing currents over a long period of time result in drying of bearings and thus failure in the motor [15].

Rotor ground currents: These currents occur when the motor is grounded via the connected load. The part of the overall ground current may pass as rotor ground current via the bearing of the motor – conductive coupling – bearing of the driven load. The magnitude of these currents depends upon the high frequency grounding impedances of stator housing and rotor, and harmful to the motor and load bearings [20].

1.3 State of the art

The common solution for mitigating the high frequency parasitic effects is the use of output filters [12]-[17]. An overview of the various output filter solutions, commonly employed in industrial applications, is presented in [14].

High frequency common mode filters, as the name indicates, reduce the high frequency noise in the motor cable. They reduce the bearing stress by limiting HF components. The cut off frequency of these filters is above the switching frequency, so the CM component at the switching frequency will be present. These filters are used in applications with unshielded cables and also for reduction of the HF emissions from the motor cable. The advantage with these filters is they do not interfere with the control of the drive so the dynamic performance of the drive is not affected [14].

Dv/dt filters are differential mode filters and have the cut-off frequency above the switching frequency [14], [15]. These filters increase the rise and fall time of the voltages and there by voltage peaks are reduced. The *dv/dt* filters protect the motor insulation. High frequency noise is caused by the switching of semiconductors. The use of *dv/dt* filters reduces the ringing oscillations frequency below 150 kHz [17]. This filter does not reduce the common mode voltage and so the bearing stress is not eliminated [16]. These filters have low reactance and are cheaper compare to sine-wave EMC filters. The applications of these filters are given in [14], [16].

The sine-wave EMC filters have the cut off frequency below the switching frequency and above the highest fundamental frequency [14]. For sine-wave EMC filters, the ringing oscillations are largely eliminated, and the motor is fed by a sinusoidal phase voltage [17]. The voltages between a line to line and line to ground are nearly sinusoidal [16]. These filters completely eliminate the bearing damage and the additional losses in the frequency converter [16]. Because of the high inductor *L* and capacitor *C*, these filters have a poor dynamic characteristic and cannot be used universally [16]. The applications of the Sine-wave EMC filters are given in [19].

HF parasitic effects in electrical drives with long cables are studied in [76] and some reduction methods are also proposed. The other solutions used in the literature to mitigate

the high frequency parasitic effects are use of damping circuits [25], matching the cable and motor input impedance [26], better winding insulations, modified modulation techniques for CM voltage reduction [27], [28] and soft gate drive techniques etc. The resonant converters can also provide solutions for reducing the voltage gradients [46]. For a motor-friendly application, the soft switching converters are investigated in this work.

1.4 Proposed system

In the literature [5], [29]-[43], [45], the reduction of switching losses can be provided with resonant converters. The resonant circuits are the combination of passive elements or passive and active elements. But the main operating principle of these converters is to bring the low voltage across and/or low current through semiconductor devices during the switching status change. There by the switching losses in the resonant converters are reduced. The rising and falling of the voltage and currents can also be controlled to reduce the ringing effects.

In resonant switch converters, the zero current or voltage is achieved by addition of resonant elements to the switch [5]. For some resonant converters, load is part of the resonant circuit. These are called load resonant converters and are located on the load side of the converter [45], [5]. For resonant DC-link converters, resonant circuit is located near to the DC-link side. Here, the zero switching loss is attained by making the dc bus oscillatory [29]-[43]. The advantage is that one resonant circuit is sufficient for soft switching of all inverter bridge switches. The problem with some resonant DC-link converters is that PWM cannot be used. In this case, the switching instants are determined by the resonant circuit [29], [30]. Some other modulation techniques have to be applied. For some resonant DC-link converters, the resonant circuit is not continuously oscillating. Whenever a switching is needed, the resonant circuit is initiated by active components. These converters are called quasi resonant DC-link converters and are capable of pulse width modulation (PWM) [31]-[43]. For motor-friendly inverter application, these types of converters are suitable due to the improved voltage spectrum.

For the switching loss reduction, *dv/dt* limitation and PWM implementation, different resonant DC-link topologies are already compared in literature [46], [47]. In this thesis, a method to reduce the CM voltage in quasi resonant DC-link (QRDCL) inverters is proposed. This method of common mode voltage reduction is possible only when the inverter is completely separated from DC-link voltage. The quasi resonant circuit must also provide variable zero voltage duration. The selected circuits in [46], [47] cannot allow the complete separation of DC-link from the inverter during resonant operation. The implemented resonant circuit in [46], [47] provides DC-link separation but shoot through state in the inverter bridge is required during resonant operation [43]. This circuit in [43] is investigated in this thesis along with another resonant circuit [41], which does not require the shoot through state. A modified pulse width modulation (PWM) is applied to the inverter. This modulation strategy together with the resonant circuit reduces the CM voltage and utilizes the maximum of available modulation index.

In resonant cycle's zero voltage duration, the resonant inductor current of [41] and [43] free wheels through the resonant switches and inverter switches respectively. So the considerable part of the stored energy in the inductor is wasted as conduction losses. A quasi resonant DC link circuit with loss less variable zero voltage duration is proposed in this thesis. This circuit provides soft switching, capable of PWM operation, *dv/dt* limitation, reduced CM voltage and loss less variable zero voltage duration in a resonant cycle.

1.5 Scope of the thesis

In chapter 2, the design procedure is given for the selected two quasi resonant DC-link inverters. These converters are modified for CM voltage reduction. They are simulated and compared. In chapter 3, the semiconductor device selection is discussed. Hardware implementation is also given. The FPGA firmware implementation of the QRDCL inverter along with the induction motor is discussed. In chapter 4, one of the selected QRDCL inverters is implemented and tested. In chapter 5, a new QRDCL inverter with loss less variable zero voltage duration is proposed. Finally, the conclusions are given in chapter 6.

The research work concerning the subsections 3.2.1 and 3.2.3 was done in a close cooperation between Mr. Calin Purcarea and me. The research topic of Mr. Purcarea [76] merged with mine in the frame of the DFG research group FOR575, 2nd phase regarding "Motor friendly and high efficient electric converters". Under the supervision of both Mr. Purcarea and mine, the work from a diploma thesis no: DA1347 [62] from our institute comprises:

- Investigation of semiconductor types for a QRDCL operation (subsection 3.2.1).
- Realization of the hardware-setup (power part) for a QRDCL converter (subsection 3.2.3).

2 Analysis and Design of Quasi-resonant DC-Link Inverters

2.1 Introduction

In the literature, there are several different types of resonant converters enabling soft zero voltage switching (ZVS) of inverter states. Quasi-resonant DC-link inverters (QRDCLI) are one type of soft switching inverters that can be controlled by pulse width modulation (PWM). The word quasi-resonant indicates that these circuits are not continuously oscillating, but can be triggered by active components to perform a resonant cycle [45]. These converters can provide zero voltage intervals during a resonant cycle. There are several quasi resonant converters mentioned in the literature [31]-[44]. These inverters can be designed not only for the soft switching but also for the voltage gradient reduction. In addition to switching loss reduction, the resonant circuit undertakes the filter's task of reducing voltage overshoot at motor terminals. A second task for the quasi-resonant inverter is the reduction of common mode (CM) voltage. This is achieved by adding an additional switch to the resonant circuit and completely separating the DC-link from the inverter bridge, which will be detailed later in this chapter. In previous topologies the common mode voltage in the case of a zero voltage vector is $\pm V_{dc}/2$. This is now reduced. The remaining values are $\pm V_{dc}/6$. The slope and level of the common mode voltage are reduced. In this way, inverter output filter functions are incorporated into a single inverter topology.

The complete separation of DC-link from the inverter bridge is not possible for the converters [31]-[38]. The quasi-resonant dc link converters in [39], [41] use more than two auxiliary switches. Reducing the number of auxiliary switches increases the efficiency of an inverter and decreases the inverter cost. The circuit presented in [42] requires a large capacitor for resonant operation, which keeps a nearly constant voltage during the resonant cycle and the energy of the resonant circuit is not zero in the steady state. The resonant circuit presented in [43] needs only two additional switches and makes all the switches in the power converter operate with zero switching losses. The energy of the resonant circuit is zero in a steady state.

The circuits presented in [41] and [43] are discussed in this chapter. These two topologies are thoroughly examined and compared. The selection of the passive component values to meet specific design criteria is also given. A method to reduce the level of the common mode voltage is discussed in detail. A modified space vector PWM (SVPWM) technique is adopted for better utilization of DC-link voltage.

2.2 The parallel three switch quasi-resonant circuit (Topology T1)

The parallel quasi-resonant dc link inverter is presented in [41], together with the differential equations and their solutions for each mode. A control expression regarding the selection of trip currents for case 1 only is presented in [41].

In this section, the differential equations and their solutions are given for each mode of operation. The expressions to calculate the trip currents for all the cases are derived here. Furthermore, the selection of appropriate passive components is also discussed here. The quasi-resonant dc link inverter is designed not only for the soft switching but also for the voltage gradient control.

The parallel quasi resonant DC link inverter shown in Figure 2.1 is presented in [41]. It will be further called as topology "T1". To simplify the illustrations of operations of this circuit, the following assumptions are made:

- The load side inductor is much larger than the resonant inductor (L_r).
- The buffer capacitor is much larger than the resonant capacitor C (= $3C_S$).

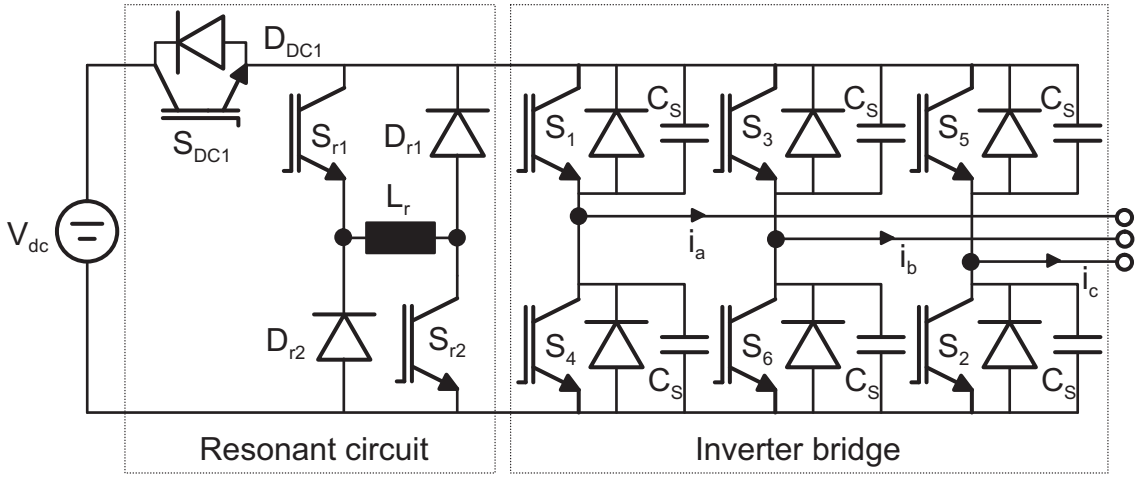


Figure 2.1 Quasi-resonant topology

- All components are ideal.

The simplified circuit used in the analysis is shown in Figure 2.3, where the converter is represented by ideal current source I_O and equivalent switch S_{INV} and diode D_{INV}. To turn on the equivalent switch S_{INV} means to turn on both the switches in one of the inverter legs simultaneously. The diode D_{INV} is conducting means both the diodes in one of the inverter legs are conducting. The equivalent current source I_O is the current flowing to the inverter during the switching period. The magnitude and direction of the current source depends upon the individual phase currents and status of six inverter switches ([39] and [40]).

$$I_O = S_1 i_a + S_3 i_b + S_5 i_c \tag{2.1}$$

$$I_{OX} = S_{1X} i_a + S_{3X} i_b + S_{5X} i_c \tag{2.2}$$

Where S_1, S_3, S_5 are the Boolean variables of the upper switches, which correspond to '0' or '1' depending upon the state of the inverter switches. A conducting switch corresponds to '1', and an off-state switch corresponds to '0'. S_{1X}, S_{3X}, S_{5X} are the next switching states after completion of a resonant operation. The three phase currents (i_a, i_b, i_c) are assumed constant during each resonant interval. The inverter input current I_O may change its value and direction during the dc link zero voltage period due to the PWM inverter switching. Four different cases classified by the direction of load current are illustrated in Figure 2.2 ([39] and [40]).

Initially, switch S_{DC1} is conducting and switches S_{r1}, S_{r2} and S_{INV} are off. The Resonant cycle starts with the turn-on of the switches S_{r1} and S_{r2}. In Figure 2.3b, operational waveforms of the resonant circuit are shown. The different operation modes are shown in Figure 2.4.

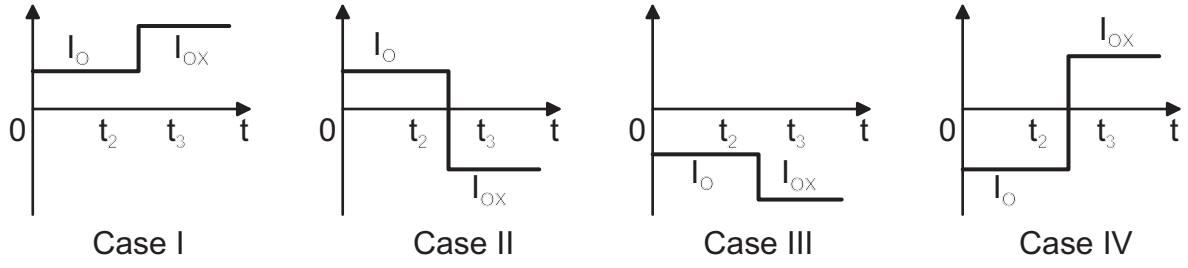


Figure 2.2 Inverter input current value and direction during zero inverter voltage period.

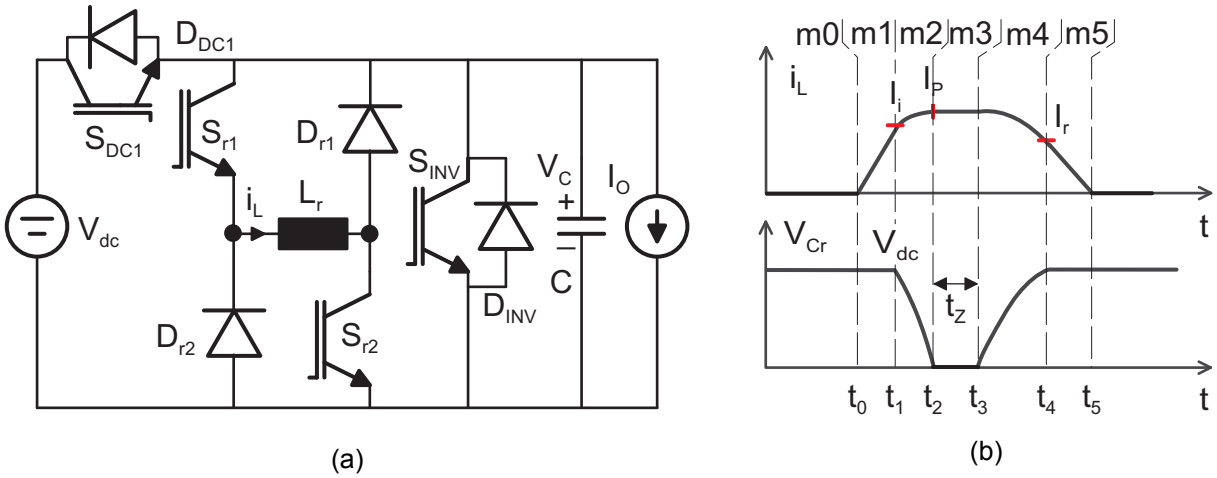


Figure 2.3 (a) Simplified circuit of the resonant converter (b) Typical waveforms

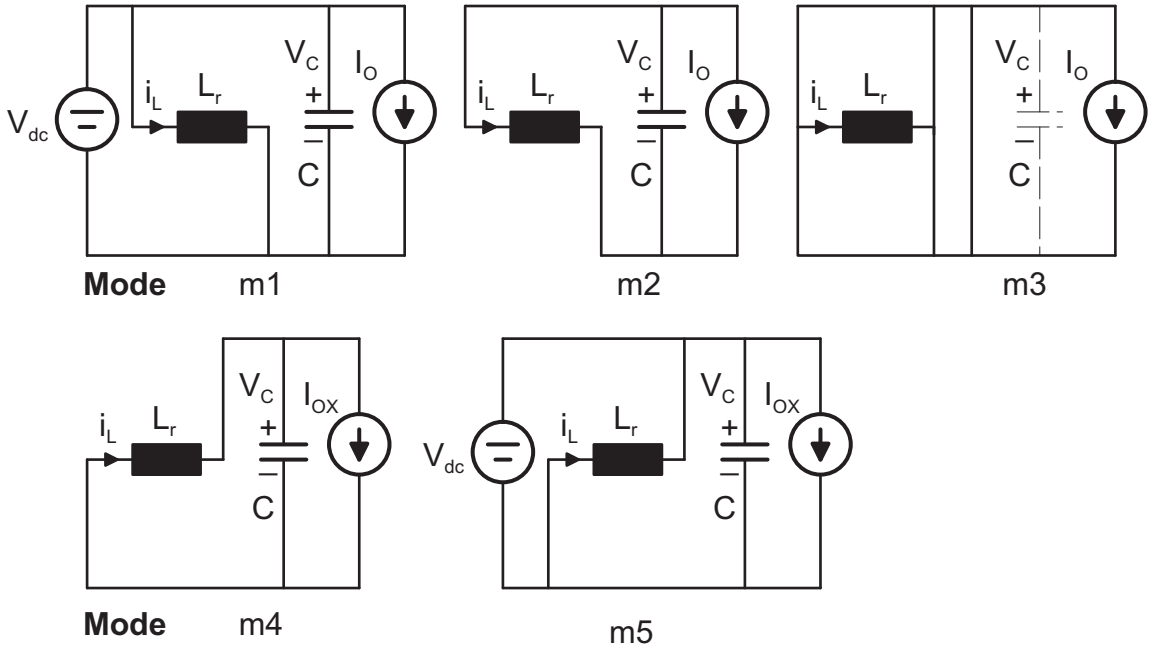


Figure 2.4 Operating modes during a resonant cycle

Mode m0 [t_0]**:** The resonant circuit is in a steady state. In the steady state, the resonant tank energy is zero, S_{DC1} is closed and S_{r1}, S_{r2}, S_{INV} are open.

$$i_L(t_0) = 0 \tag{2.3}$$

$$V_C(t_0) = V_{dc} \tag{2.4}$$

Mode m1 [t_0, t_1]**:** At a time t_0, the power devices in the PWM inverter need to be switched. Since the DC link voltage V_{dc} is not zero, the inverter power devices are not switched immediately. The switches S_{r1} and S_{r2} are closed under zero current condition. A resonant cycle is started. Thus the inductor current i_L reaches I_i at which sufficient energy is stored in the inductor.

$$i_L(t) = \frac{V_{dc}}{L_r}(t - t_0) \tag{2.5}$$

$$V_C(t) = V_{dc} \tag{2.6}$$

$$\text{At } t = t_1,\ i_L(t_1) = I_i \ \Rightarrow\ (t_1 - t_0) = \frac{L_r}{V_{dc}} I_i \tag{2.7}$$

Mode m2 [t_1, t_2]**:** When the inductor current i_L is equal to I_i, switch S_{DC1} is turned off under zero voltage condition. The DC link voltage source is disconnected from the PWM inverter. The current i_L then discharges the capacitor C and V_C falls to zero as a result of resonance between C and L_r. For given resonant elements, the maximum voltage rate of change of depends upon the trip current I_i and the value of I_O.

$$i_L(t) = \frac{V_{dc}}{Z_r}\sin\left(\omega_r(t - t_1)\right) + (I_i + I_O)\cos\left(\omega_r(t - t_1)\right) - I_O \tag{2.8}$$

$$V_C(t) = V_{dc}\cos\left(\omega_r(t - t_1)\right) - (I_i + I_O)Z_r\sin\left(\omega_r(t - t_1)\right) \tag{2.9}$$

$$\text{At } t = t_2,\ V_C(t_2) = 0 \ \Rightarrow\ i_L(t_2) = I_P = \sqrt{(I_i + I_O)^2 + \left(\frac{V_{dc}}{Z_r}\right)^2} - I_O \tag{2.10}$$

$$(t_2 - t_1) = \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_{dc}/Z_r}{(I_i + I_O)}\right) = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_{dc}}{(I_P + I_O)Z_r}\right) \tag{2.11}$$

Mode m3 [t_2, t_3]**:** When the link voltage V_{dc} reaches zero, all the upper switches or lower switches of the inverter are turned on. Then, the load current always freewheels through the inverter itself. The current i_L freewheels through the paths of S_{r1}-D_{r1} and S_{r2}-D_{r2}, but not through the inverter bridge. So the switching of both upper and lower devices is not necessary. The duration (t_3 ─ t_2) of this mode is controllable. The inverter devices change the switching state to the next one at the end of this mode. The inverter input current I_O is changed to I_{OX}, which is determined by (2.2).

$$i_L(t_2) = I_P \tag{2.12}$$

$$V_C(t_2) = 0 \tag{2.13}$$

Mode m4 [t_3, t_4]**:** The switches S_{r1} and S_{r2} are turned off under zero voltage condition. The DC link voltage V_C reaches to the buffer voltage V_{dc}. Then the switch S_{DC1} can be turned on under zero voltage condition.

$$i_L(t) = (I_P - I_{OX})\cos\left(\omega_r(t - t_3)\right) + I_{OX} \tag{2.14}$$

$$V_C(t) = (I_P - I_{OX})Z_r\sin\left(\omega_r(t - t_3)\right) \tag{2.15}$$

$$\text{At } t = t_2,\ V_C(t_4) = V_{dc} \ \Rightarrow\ i_L(t_4) = I_r = \sqrt{(I_P - I_{OX})^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} + I_{OX} \tag{2.16}$$

$$(t_4 - t_3) = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_{dc}/Z_r}{(I_P - I_{OX})}\right) = \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_{dc}/Z_r}{(I_r - I_{OX})}\right) \tag{2.17}$$

Mode m5 [t_4, t_5]**:** The remaining energy in the resonant inductor is returned to the voltage source. The inductor current i_L decreases linearly to zero.

$$i_L(t) = -\frac{V_{dc}}{L_r}(t - t_4) + I_r \tag{2.18}$$

$$V_C(t) = V_{dc} \tag{2.19}$$

$$(t_5 - t_4) = \frac{L_r}{V_{dc}} I_r \tag{2.20}$$

2.2.1 Calculation of the Trip current

Case I: (Figure 2.2)

In this case, the inverter input current before switching and also after switching is positive. It does not change its direction during the DC link voltage interval mode m3 [t_2, t_3]. From mode m2 and m4, the equations are represented here again.

$$\text{From (2.10), } I_P = \sqrt{(I_i + I_O)^2 + \left(\frac{V_{dc}}{Z_r}\right)^2} - I_O \tag{2.21}$$

$$\text{From (2.11), } (t_2 - t_1) = \frac{1}{\omega_r} \sin^{-1}\left(\frac{V_{dc}}{(I_P + I_O) Z_r}\right) \tag{2.22}$$

$$\text{From (2.16), } I_r = \sqrt{(I_P - I_{OX})^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} + I_{OX} \tag{2.23}$$

$$\text{From (2.17), } (t_4 - t_3) = \frac{1}{\omega_r} \cos^{-1}\left(\frac{I_r - I_{OX}}{I_P - I_{OX}}\right) \tag{2.24}$$

The constraints $(t_2 - t_1) \geq 0$ and $(t_4 - t_3) \geq 0$ for (2.22) and (2.24) respectively lead to the following inequalities:

$$0 \leq \sin\left(\omega_r (t_2 - t_1)\right) \leq 1 \Rightarrow 0 \leq \frac{V_{dc}}{(I_P + I_O) Z_r} \leq 1 \Rightarrow I_P \geq \frac{V_{dc}}{Z_r} - I_O \tag{2.25}$$

$$0 \leq \cos\left(\omega_r (t_4 - t_3)\right) \leq 1 \Rightarrow 0 \leq \frac{I_r - I_{OX}}{I_P - I_{OX}} \leq 1 \Rightarrow I_{OX} \leq I_r \leq I_P \tag{2.26}$$

The current I_r is the residual inductor current $i_L(t_4)$. At the end of the mode m4, the voltage V_C recharges to V_{dc}. At this moment, the inductor should be able to supply the load current I_{OX}. If this inductor current I_r is less than the load current, the capacitor C will start discharging until the switch S_{DC1} is turned on again (m1). So the minimum value of the residual inductor current I_r is I_{OX}. At the end of the mode m4, the switch S_{DC1} is closed and the residual current I_r flows through the diode D_{DC1} and back to the dc link voltage (m5). Here, the voltage V_C is clamped to V_{dc}.

For the minimum value of I_r from (2.26) and applying it into (2.23) yields,

$$I_r = \sqrt{(I_P - I_{OX})^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} + I_{OX} \geq I_{OX} \;\Rightarrow\; I_P \geq \frac{V_{dc}}{Z_r} + I_{OX} \tag{2.27}$$

From (2.25) and (2.27),

$$I_P \geq \frac{V_{dc}}{Z_r} + I_{OX} \tag{2.28}$$

By applying (2.28) into (2.21), the condition for the trip current I_i results for the case I (Figure 2.2):

$$I_i \geq \sqrt{\left(\frac{V_{dc}}{Z_r} + I_O + I_{OX}\right)^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} - I_O \tag{2.29}$$

Case II:

In this case, the inverter input current changes its direction. The inverter input current changes its direction from positive value (I_O) to negative value ($-I_{OX}$) during the DC link voltage interval mode m3 [t_2, t_3]. The equations derived for each mode of the case I are valid for case II, when I_{OX} is replaced with a negative sign.

The constraints for case II are as follows:

$$0 \leq \sin\left(\omega_r\left(t_2 - t_1\right)\right) \leq 1 \Rightarrow 0 \leq \frac{V_{dc}}{\left(I_P + I_O\right)Z_r} \leq 1 \Rightarrow I_P \geq \frac{V_{dc}}{Z_r} - I_O \tag{2.30}$$

$$0 \leq \cos\left(\omega_r\left(t_4 - t_3\right)\right) \leq 1 \Rightarrow 0 \leq \frac{I_r + I_{OX}}{I_P + I_{OX}} \leq 1 \Rightarrow -I_{OX} \leq I_r \leq I_P \tag{2.31}$$

For case II, the minimum value of the residual inductor current I_r is $-I_{OX}$. The value I_r cannot be negative. The minimum value for I_r is taken as zero. At the end of the mode m4, I_r is zero and the load current I_{OX} flows through the diode D_{DC1} and back to the dc link voltage (m5). Here, the voltage V_C is clamped to V_{dc}.

$$I_r \geq 0 \;\Rightarrow\; I_P \geq \sqrt{\left(I_{OX}\right)^2 + \left(\frac{V_{dc}}{Z_r}\right)^2} - I_{OX} \tag{2.32}$$

Both the equations (2.30) and (2.32) are to be satisfied. The minimum value for current I_P is the minimum current that satisfies both the equations. From this value of peak current I_P, the trip current I_i is calculated for case II.

$$I_i = \sqrt{\left(I_P + I_O\right)^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} - I_O \tag{2.33}$$

Case III:

In this case, the inverter input current before switching and also after switching is negative. It does not change its direction during the DC-link voltage interval mode m3 [t_2, t_3]. The equations derived for each mode in case I are also valid for case III, when I_O and I_{OX} are replaced with negative signs.

The constraints for case III are as follows:

$$0 \leq \sin\left(\omega_r\left(t_2 - t_1\right)\right) \leq 1 \Rightarrow 0 \leq \frac{V_{dc}}{\left(I_P - I_O\right)Z_r} \leq 1 \Rightarrow I_P \geq \frac{V_{dc}}{Z_r} + I_O \tag{2.34}$$

$$0 \leq \cos\left(\omega_r\left(t_4 - t_3\right)\right) \leq 1 \Rightarrow 0 \leq \frac{I_r + I_{OX}}{I_P + I_{OX}} \leq 1 \Rightarrow -I_{OX} \leq I_r \leq I_P \tag{2.35}$$

As in case II, the minimum value for I_r is also taken as zero for case III. Then,

$$I_r \geq 0 \;\Rightarrow\; I_P \geq \sqrt{\left(I_{OX}\right)^2 + \left(\frac{V_{dc}}{Z_r}\right)^2} - I_{OX} \tag{2.36}$$

Both the equations (2.34) and (2.36) are to be satisfied. The minimum value for current I_P is the minimum current that satisfies both the equations. From this value of peak current I_P, the trip current I_i is calculated for case III.

$$I_i = \sqrt{\left(I_P - I_O\right)^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} + I_O \tag{2.37}$$

Case IV:

In this case, the inverter input current changes its direction from negative to positive value during the DC link voltage interval mode m3 [t_2, t_3]. The equations derived for each mode of case I are valid for case II, when I_O is replaced with a negative sign.

The constraints for the case IV are as follows:

$$0 \leq \sin\left(\omega_r\left(t_2 - t_1\right)\right) \leq 1 \Rightarrow 0 \leq \frac{V_{dc}}{\left(I_P - I_O\right)Z_r} \leq 1 \Rightarrow I_P \geq \frac{V_{dc}}{Z_r} + I_O \tag{2.38}$$

$$0 \leq \cos\left(\omega_r\left(t_4 - t_3\right)\right) \leq 1 \Rightarrow 0 \leq \frac{I_r - I_{OX}}{I_P - I_{OX}} \leq 1 \Rightarrow I_{OX} \leq I_r \leq I_P \tag{2.39}$$

The minimum value for I_r is I_{OX} for the case IV. Then,

$$I_r = \sqrt{\left(I_P - I_{OX}\right)^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} + I_{OX} \geq I_{OX} \;\Rightarrow\; I_P \geq \frac{V_{dc}}{Z_r} + I_{OX} \tag{2.40}$$

Both the equations (2.38) and (2.40) are to be satisfied. The minimum value for current I_P is the minimum current that satisfies both the equations. From this value of peak current I_P, the trip current I_i is calculated for case III.

$$I_i = \sqrt{\left(I_P - I_O\right)^2 - \left(\frac{V_{dc}}{Z_r}\right)^2} + I_O \tag{2.41}$$

The trip currents calculated above does not take care of the losses. So the actual trip current must be greater than these calculated values. Figure 2.7 shows the relation between the minimum trip current I_i, present load current I_O and next load current I_{OX} graphically for the parameters selected in the section 2.2.2.

2.2.2 Design Considerations

First, the most important design objective is that inverter input voltage must be pulled down to zero for zero voltage switching (ZVS) and again boosted to the DC-link source voltage. Second, it is important to minimize the peak value of the resonant current in order to reduce the stress on circuit devices. This peak current (I_P) increases with an increase of the inverter bridge input current (I_O or I_{OX}). Third, the rising and falling slope of the inverter output voltage must be low for long cable drives. The capacitor C will be discharged quickly with high I_O. The capacitor C will be charged quickly with high I_{OX}. To get the quantitative feeling, these values for all the cases are presented in Table 2.1. The values chosen for resonant inverter circuit are V_{dc} = 540 V, L_r = 30 µH, C = 0.15 µF.

Table 2.1: A design example

	Case I I_O = 22, I_{OX} = 22	Case II I_O = 22, I_{OX} = -22	Case III I_O = -22, I_{OX} = -22	Case IV I_O = -22, I_{OX} = 22
I_i	50.78 A	0 A	22 A	22 A
I_P	**60.18 A**	22.07 A	**60.18 A**	**60.18 A**
$t_2 - t_1$	**1.03 µs**	2.22 µs	3.33 µs	3.33 µs
$t_4 - t_3$	3.33 µs	2.22 µs	**1.03 µs**	3.33 µs

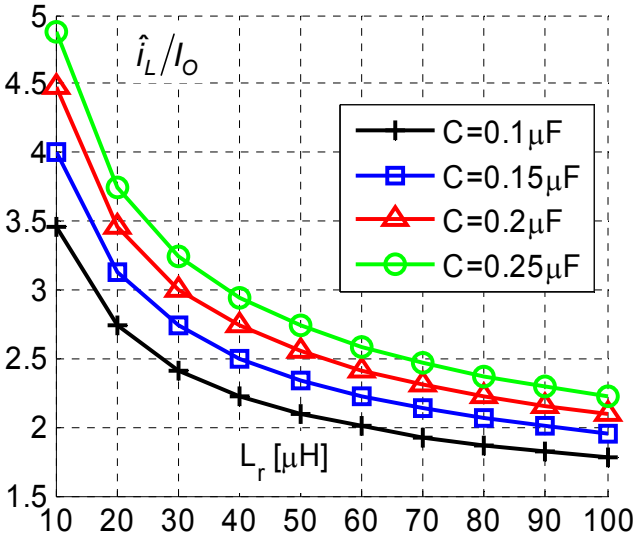


Figure 2.5 Peak values of normalized current (i_L) for V_{dc} = 540 V, I_O = I_{OX} = 22 A.

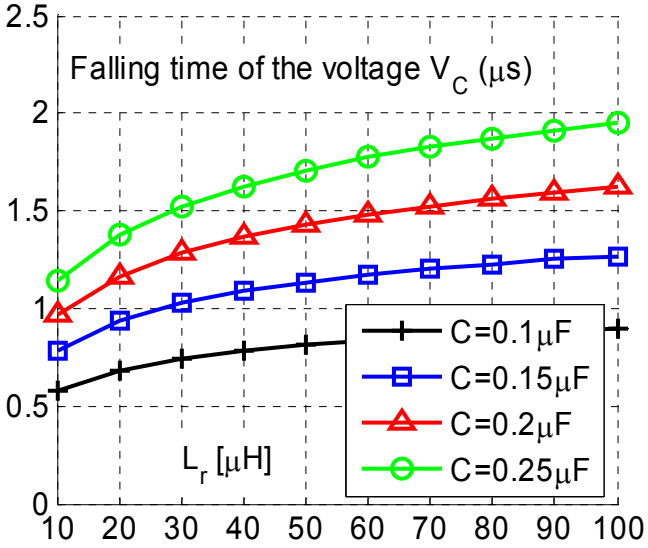


Figure 2.6 Falling times of voltage V_C for V_{dc} = 540 V, I_O = I_{OX} = 22 A.

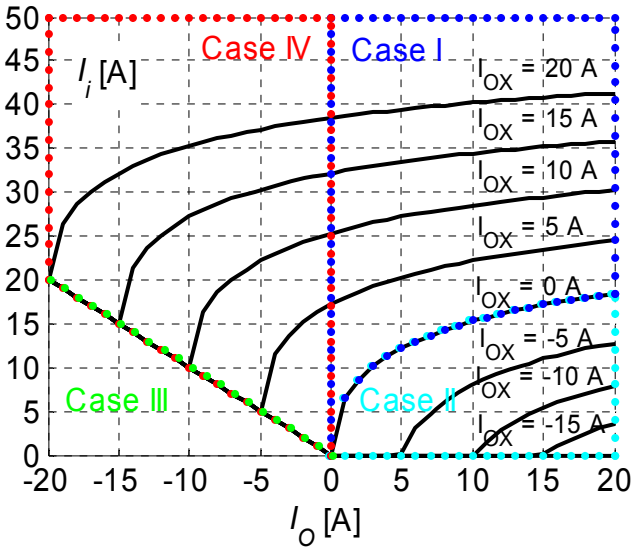


Figure 2.7 The variation in trip current I_i according to the present load current I_O and next load current I_{OX}

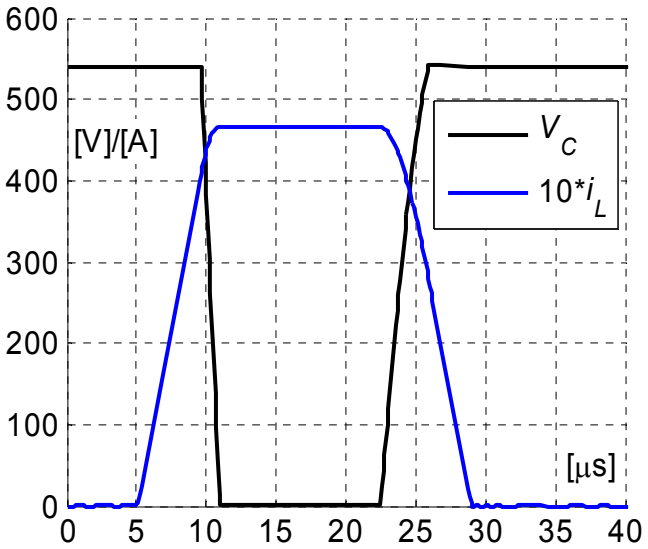


Figure 2.8 Simulation waveforms

From Table 2.1, it is concluded that peak current (I_P) and the falling time of the voltage ($t_2 - t_1$) of case I together determine the resonant link passive components (L_r and

C). The equations for peak current through the inductor (I_P) and falling time of the voltage ($t_2 - t_1$) are given in (2.10), (2.11). Figure 2.5 shows the normalized maximum positive peak current of the resonant inductor i_L according to the inductor L_r for each capacitor *C*. Figure 2.6 shows the variation of the falling time of the voltage V_C for different values of L_r and *C*.

The converter is designed to achieve the maximum voltage gradient of 600 *V/µs* and simultaneously to have low peak current and voltage stresses on the devices and thereby to reduce the losses. The selected parameters for the converter are as follows: Resonant Inductor L_r = 60 µH and capacitor *C* = 0.15 µF. The trip currents (I_i) for the selected parameters are given in Figure 2.7. A simulation model for resonant converter has been developed and implemented in Simplorer® network simulation software. In Figure 2.8, the simulated waveforms for resonant circuit are shown.

2.3 The parallel two switch quasi-resonant circuit (Topology T2)

This quasi resonant dc link inverter is presented in [43], together with the differential equations. The selection of trip currents is not discussed in [43], [44].

In this section, the differential equations and their solutions are given for each mode of operation. The expressions to calculate the trip currents for all the cases are derived here. Furthermore, the selection of appropriate passive components is also discussed here.

The quasi resonant DC-link circuit in [43] is presented in Figure 2.9. It will be further called as topology "T2". The resonant circuit needs only two additional switches and makes all the switches in the inverter bridge operate with zero switching losses. The energy of the resonant circuit is zero in the steady state. To simplify the descriptions of operations of this circuit, the assumptions given in section 2.2 are also valid here.

For a switching period, the simplified equivalent circuit is as shown in Figure 2.10a. The six switches of the bridge are represented by a single switch S_{INV} for the purpose of the analysis. The equivalent current source I_O represents the inverter's DC-link current whose value and direction depend on the individual phase currents of the machine and the status of inverter switches ([39] and [40]).

Initially, switch S_{DC1} is conducting and switches S_r and S_{INV} are off. The Resonant cycle starts with the turn-on of the switch S_r. In Figure 2.10b, operational waveforms of the resonant circuit are shown. The different operation modes are shown in Figure 2.11.

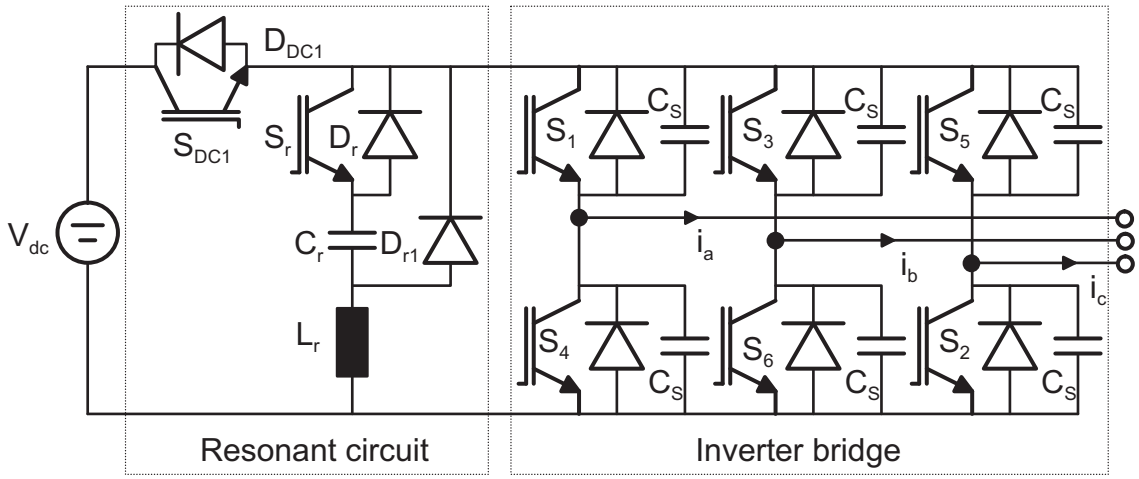


Figure 2.9 Quasi-resonant topology

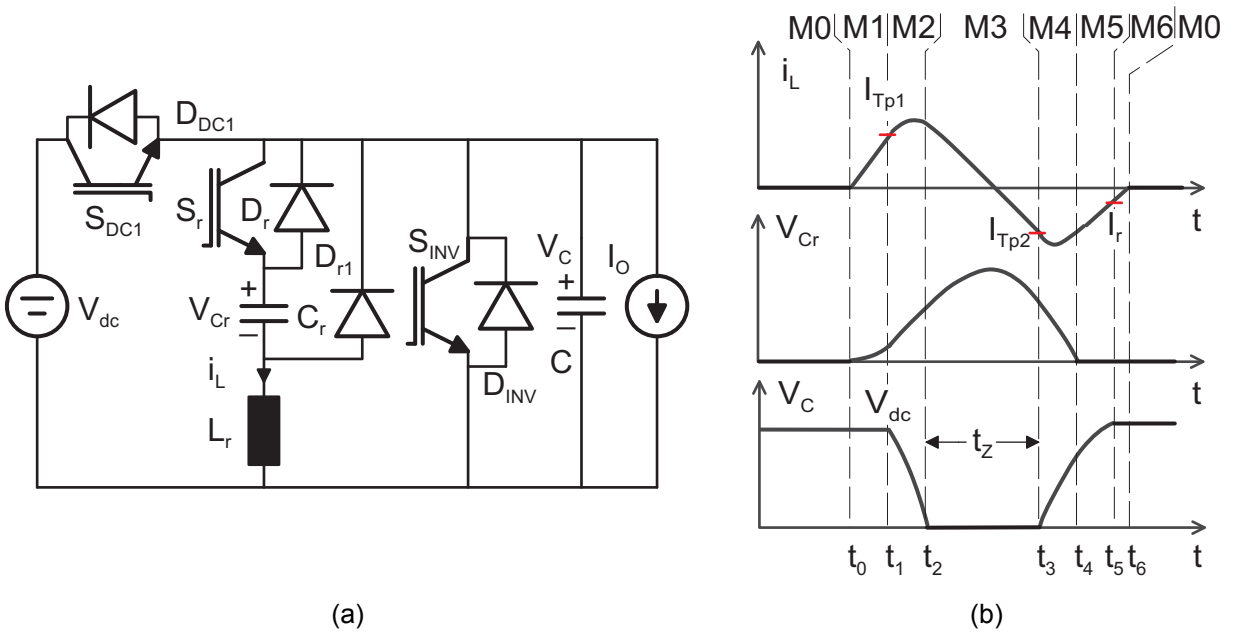


Figure 2.10 (a) Simplified circuit of the resonant converter (b) Typical waveforms

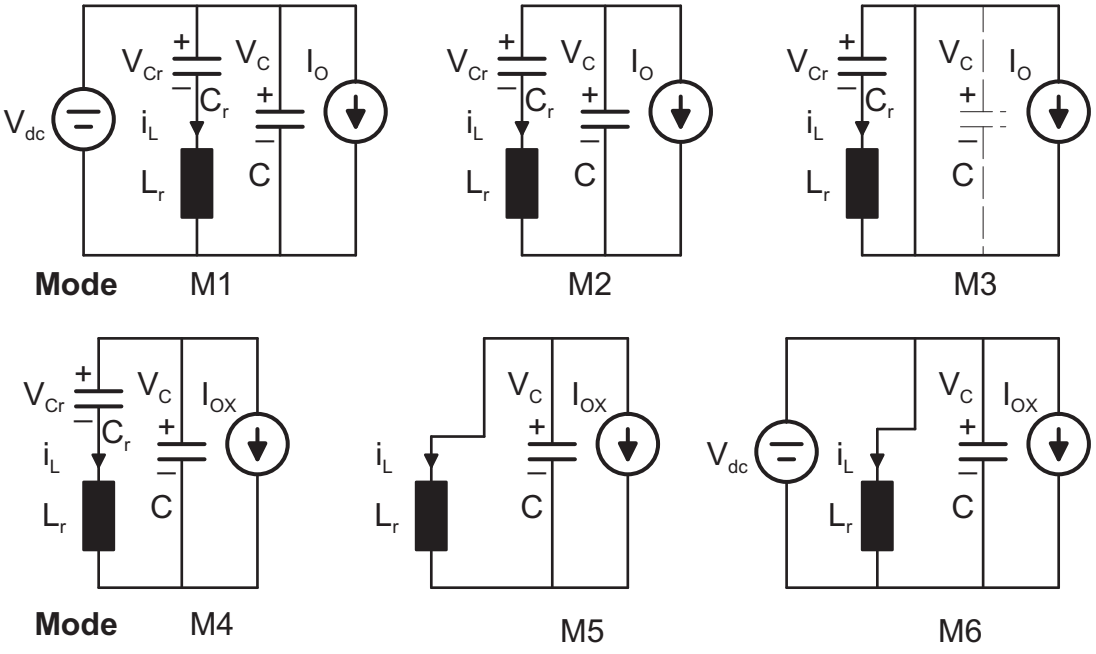


Figure 2.11 Operating modes during a resonant cycle

The following notations will be used in the subsequent equations:

$$C_{sum} = C + C_r, a = \frac{C_r}{C_{sum}}, b = \frac{C}{C_{sum}}, \omega_0 = \frac{1}{\sqrt{L_r C_r}}, \omega_1 = \sqrt{\frac{C + C_r}{LCC_r}}, \omega_2 = \frac{1}{\sqrt{L_r C}},$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}}, Z_1 = \frac{1}{\omega_1 C}, Z_2 = \omega_1 L, Z_3 = \frac{1}{\omega_1 C_r}, Z_4 = \frac{1}{\omega_1 C_{sum}}, Z_5 = \sqrt{\frac{L_r}{C}}$$

Mode M0 [t_0]**:** The resonant circuit is in the steady state. In the steady state, the resonant tank energy is zero, S_{DC1} is closed and S_r is open.

$$i_L(t_0) = 0 \tag{2.42}$$

$$V_{Cr}(t_0) = 0 \tag{2.43}$$

$$V_C(t_0) = V_{dc} \tag{2.44}$$

Mode M1 [t_0, t_1]**:** At a time t_0, power devices in the PWM inverter need to be switched. Since the DC link voltage V_C is not zero, the inverter power devices are not switched immediately. The switch S_r is turned-on under zero current condition. By turning S_r on, a resonant cycle is started. Thus the inductor current i_L reaches I_{Tp1} at which sufficient energy is stored in an inductor.

$$\theta = \omega_0 (t - t_0)$$

$$i_L(t) = \frac{V_{dc}}{Z_0} \sin\theta \tag{2.45}$$

$$V_{Cr}(t) = V_{dc}(1 - \cos\theta) \tag{2.46}$$

$$V_C(t) = V_{dc} \tag{2.47}$$

$$\text{At } t = t_1, i_L(t_1) = I_{Tp1} \;\Rightarrow\; \sin\theta = \frac{I_{Tp1} Z_0}{V_{dc}} \;\Rightarrow\; \cos\theta = \frac{\sqrt{V_{dc}^2 - (I_{Tp1} Z_0)^2}}{V_{dc}} \tag{2.48}$$

$$\text{At } t = t_1, V_{Cr}(t_1) = V_{dc}(1 - \cos\theta) = V_{dc} - \sqrt{V_{dc}^2 - (I_{Tp1} Z_0)^2} \tag{2.49}$$

Mode M2 [t_1, t_2]**:** When the inductor current i_L is equal to I_{Tp1}, switch S_{DC1} is turned off under zero voltage condition. The DC link voltage source is disconnected from the PWM inverter. The current i_L then discharges the capacitor C and V_C falls to zero as a result of resonance between C, C_r and L_r. For given resonant elements, the maximum voltage rate of change of depends upon the selection of the trip current I_{Tp1} and value of I_O.

$$\theta = \omega_1 (t - t_1)$$

$$i_L(t) = (aI_O + i_L(t_1))\cos\theta + \frac{V_{dc} - V_{Cr}(t_1)}{Z_2} \sin\theta - aI_O \tag{2.50}$$

$$V_{Cr}(t) = b(V_{Cr}(t_1) - V_{dc})\cos\theta + Z_3(aI_O + i_L(t_1))\sin\theta + bV_{dc} + aV_{Cr}(t_1) - \frac{I_O(t - t_1)}{C_{sum}} \tag{2.51}$$

$$V_C(t) = a(V_{dc} - V_{Cr}(t_1))\cos\theta - Z_1(aI_O + i_L(t_1))\sin\theta + bV_{dc} + aV_{Cr}(t_1) - \frac{I_O(t - t_1)}{C_{sum}} \tag{2.52}$$

$$\text{At } t = t_2, V_C(t_2) = 0 \Rightarrow V_{Cr}(t_2) = \frac{Z_2}{Z_1}\left(V_{dc} - a\sqrt{V_{dc}^2 - (I_{Tp1} Z_0)^2} - \frac{I_O(t - t_1)}{C_{sum}}\right) \tag{2.53}$$

$$i_L(t_2)=\sqrt{\frac{V_{dc}^2-\left(I_{Tp1}Z_0\right)^2}{Z_2^2}+\left(aI_O+i_L(t_1)\right)^2-\left(\frac{V_{Cr}(t_2)}{Z_2}\right)^2}-aI_O \tag{2.54}$$

Mode M3 [t_2, t_3]**:** When the link voltage V_C reaches zero, all power devices in the inverter are turned on. In terms of the simplified equivalent circuit, S_{INV} is turned on under zero voltage condition. So the link voltage V_C remains zero. Due to resonance between C_r and L_r, the inductor current i_L changes its direction. Therefore, switch S_r is turned off under zero voltage and zero current condition.

$$\theta=\omega_0(t-t_2)$$

$$i_L(t)=i_L(t_2)\cos\theta-\frac{V_{Cr}(t_2)}{Z_0}\sin\theta \tag{2.55}$$

$$V_{Cr}(t)=V_{Cr}(t_2)\cos\theta+Z_0 i_L(t_2)\sin\theta \tag{2.56}$$

$$V_C(t)=0 \tag{2.57}$$

Mode M4 [t_3, t_4]**:** When the inductor current i_L is equal to second trip current I_{Tp2}, switch S_{INV} is turned off under zero voltage condition. That means a new switching status is applied to the inverter under ZVS condition. The capacitor voltage V_{Cr} falls to zero as a result of resonance between C, C_r and L_r. Diode D_{r1} begins to conduct.

$$\theta=\omega_1(t-t_3)$$

$$i_L(t)=\left(aI_O+i_L(t_3)\right)\cos\theta-\frac{V_{Cr}(t_3)}{Z_2}\sin\theta-aI_{OX} \tag{2.58}$$

$$V_{Cr}(t)=bV_{Cr}(t_3)\cos\theta+Z_3\left(aI_O+i_L(t_3)\right)\sin\theta+aV_{Cr}(t_3)-\frac{I_{OX}(t-t_3)}{C_{sum}} \tag{2.59}$$

$$V_C(t)=aV_{Cr}(t_3)(1-\cos\theta)-Z_1\left(aI_{OX}+i_L(t_3)\right)\sin\theta-\frac{I_{OX}(t-t_3)}{C_{sum}} \tag{2.60}$$

$$\text{At } t=t_4, V_{Cr}(t_4)=0\Rightarrow V_C(t_4)=\frac{Z_2}{Z_3}\left(aV_{Cr}(t_3)-\frac{I_{OX}(t-t_3)}{C_{sum}}\right) \tag{2.61}$$

$$i_L(t_4)=\sqrt{\left(aI_{OX}+i_L(t_3)\right)^2+\left(\frac{V_{Cr}(t_3)}{Z_2}\right)^2-\left(\frac{V_C(t_4)}{Z_2}\right)^2}-aI_{OX} \tag{2.62}$$

Mode M5 [t_4, t_5]**:** In this mode, resonance between C and L_r takes place. The inverter voltage V_C reaches to the dc link voltage V_{dc}. Then the switch S_{DC1} can be turned on under zero voltage condition.

$$\theta=\omega_2(t-t_4)$$

$$i_L(t)=\left(i_L(t_4)+I_{OX}\right)\cos\theta+\frac{V_C(t_4)}{Z_5}\sin\theta-I_{OX} \tag{2.63}$$

$$V_{Cr}(t) = 0 \tag{2.64}$$

$$V_C(t) = V_C(t_4)\cos\theta - Z_5\left(I_{OX} + i_L(t_4)\right)\sin\theta \tag{2.65}$$

$$\text{At } t = t_4, V_C(t_5) = V_{dc} \Rightarrow i_L(t_5) = -\sqrt{\left(I_{OX} + i_L(t_4)\right)^2 + \left(\frac{V_C(t_4)}{Z_5}\right)^2 - \left(\frac{V_{dc}}{Z_5}\right)^2} - I_{OX} \tag{2.66}$$

Mode M6 [t_5, t_6]**:** The inductor current i_L goes back to zero from a negative value. The sub circuit is shown in Figure 2.11.

$$i_L(t) = i_L(t_5) + \frac{V_{dc}}{L_r}(t - t_5) \tag{2.67}$$

$$V_{Cr}(t) = 0 \tag{2.68}$$

$$V_C(t) = V_{dc} \tag{2.69}$$

2.3.1 Calculation of the Trip currents

The resonant elements also produce losses during resonant operation. So the stored energy in these resonant elements for the resonant operation should be optimum. In the selected resonant circuit, the trip currents decide the stored energy. Therefore, by optimally controlling the trip currents, the efficiency of a soft switching inverter can be further improved. A simple method to calculate the minimum trip currents is presented in this section.

The aim is to calculate the trip currents I_{TP1} and I_{TP2} for all load currents such that a) at the end of a resonant cycle the DC-link voltage is restored b) the amplitudes of the resonant current are minimized. The specification (b) is necessary in order to reduce the circuit power loss and to reduce the stress on the semiconductor devices during a resonant operation and thereby improving the efficiency further. The resonant cycle is heavily influenced by the initial load current I_O and by I_{OX} at the next switching state. In order to get general results for all combinations of I_O and I_{OX}, analytical solutions for this boundary problem shall be used as far as possible.

The method was intended as follows: First for each mode, the solutions for the state variables, i.e. inductor current and capacitor voltages are derived. That is not the problem. The problem is to find the boundaries between all the modes, such that all constraints are fulfilled. This problem is illustrated for Case I.

In Case I, the inverter input current before switching and also after switching is positive. It does not change its direction during the DC link voltage interval mode M3 [t_2, t_3]. The current I_r is the residual inductor current $i_L(t_5)$ (Figure 2.10b). At the end of the mode M5, the voltage V_C recharges to V_{dc}. At this moment, the inductor should be able to supply the load current I_{OX}. If the magnitude of this inductor current I_r is less than the load current, the capacitor C will start discharging until the switch S_{DC1} is turned on again (M1). So the maximum value of residual inductor current I_r is $-I_{OX}$. At the end of mode M5, the switch S_{DC1} is closed and the residual current I_r flows through the diode D_{DC1} and back to the dc link voltage (M6). Here, the voltage V_C is clamped to V_{dc}.

For the value of $I_r = i_L(t_5) = -I_{OX}$ and applying it into (2.66) yields

$$I_r = i_L(t_5) \le -I_{OX} \quad \Rightarrow \left(I_{OX} + i_L(t_4)\right)^2 + \left(\frac{V_C(t_4)}{Z_5}\right)^2 - \left(\frac{V_{dc}}{Z_5}\right)^2 \le 0 \tag{2.70}$$

In order to solve these equations, the values of $i_L(t_4)$ and $V_C(t_4)$ are taken from (2.61) and (2.62) (mode M4), which in turn depends upon (2.55) and (2.56) (mode M3) and so on.

Equations (2.48), (2.49), (2.53), (2.54), (2.55), (2.56), (2.61), (2.62) and (2.70) are to be solved for I_{Tp1}, I_{Tp2}. An analytical solution for the trip currents turned out to be highly complicated. It is due to the complex modes and three passive elements L_r, C_r, C. Therefore, that the problem was solved in two steps:

- First, the solution is derived for a simpler resonant circuit which has only one instead of two capacitors, and simpler modes.
  The topology presented in [41] which was discussed in section 2.2 as topology 1 (T1) uses an inductor L_r and a capacitor C as resonant elements and operates in similar fashion as present topology (T2). Initially, the energy stored in resonant elements during mode m1 is calculated (section 2.2.1).

- Second, storing the same amount of energy during mode M1 of the target topology T2, allows to calculate the trip current I_{TP1}. In a similar way I_{TP2} can be found.

In both topologies, the inductors (L_r) and capacitors (C) have the same value. The energy needed to null the inverter input voltage and bring it back to the dc link voltage is same in both the topologies. In T2, the energy needed to complete a resonant cycle is stored in inductor L_r and capacitor C_r. In T1, the energy needed to complete a resonant cycle is stored in the inductor L_r only. This facilitates the simple derivation of trip current I_i for T1. The calculation of this trip current I_i for all cases is discussed in section 2.2.1.

A Trip current I_{Tp1} for topology T2

The first resonant stage occurs in mode M1. At the end of this period, the inductor current i_L reaches the value I_{Tp1}. The equations for this mode M1 are repeated here:

$$i_L(t_1) = I_{Tp1} \tag{2.71}$$

$$V_{Cr}(t_1) = V_{Cr1} = V_{dc} - \sqrt{V_{dc}^2 - \left(I_{Tp1}Z_0\right)^2} \tag{2.72}$$

For the same input currents I_O and I_{OX}, energy needed to null the inverter input voltage and bring it back to the DC-link voltage is same in both the topologies. By using the trip current I_i calculated for different cases of topology T1 and the energy balance equation (2.73), trip current I_{Tp1} is calculated in (2.74) for all cases of topology T2.

$$1/2\,C_r V_{Cr1}^2 + 1/2\,L_r I_{Tp1}^2 = 1/2\,L_r I_i^2 \tag{2.73}$$

$$I_{Tp1} = \sqrt{\left(\frac{V_{dc}}{Z_0}\right)^2 - \left(\frac{V_{dc}}{Z_0} - \frac{I_i^2 Z_0}{2V_{dc}}\right)^2} \tag{2.74}$$

Figure 2.16 shows the relation between the minimum trip current I_{Tp1}, present load current I_O and next load current I_{OX} graphically for the parameters selected in the section 2.3.2.

B *Trip current I_{Tp2} for topology T2*

The value of I_{TP2} must satisfy two needs. First the current i_L, must be large enough to ensure that the oscillation is completed and V_C reaches the supply value V_{dc}. Second, the capacitor voltage V_{Cr} must be zero at the end of a resonant cycle.

For topology T1 (Figure 2.3b), the current $i_L(t_3) = I_P$. The total energy stored in the resonant inductor is $L_r I^2_P/2$. The minimum residual current in the inductor is $i_L(t_4)_{,Min} = I_r$.

For topology T2 (Figure 2.10b), the current $i_L(t_3) = I_{Tp2}$, which is the second trip current. The total energy stored in the resonant elements is $(1/2\ C_r V_{Cr}(t_3)^2 + 1/2\ L_r I_{Tp2}^2)$. It is assumed that voltage V_C reaches the dc link voltage, and at the same time the resonant capacitor voltage V_{Cr} becomes zero. This assumption reduces the number of modes (combines M4 and M5) and helps in reducing resonant cycle duration. Then equations for the topology T2 are as follows:

$$i_L(t_3) = I_{Tp2}, V_C(t_4) = V_{dc}, V_{Cr}(t_4) = 0, i_L(t_4)_{,Min} = -I_r \tag{2.75}$$

$$1/2\, C_r V_{Cr}^2(t_3) + 1/2\, L_r I_{Tp2}^2 = 1/2\, L_r I_P^2 \tag{2.76}$$

From (2.62) and (2.75),

$$i_L(t_4) = -I_r = -\sqrt{\left(I_{Tp2} + aI_{OX}\right)^2 + \left(\frac{V_{Cr}(t_3)}{Z_2}\right)^2 - \left(\frac{V_{dc}}{Z_2}\right)^2} - aI_{OX} \tag{2.77}$$

The trip current I_{TP2} can be calculated by solving the equations (2.76) and (2.77). Figure 2.17 shows the relation between the minimum trip current I_{TP2}, present load current I_O and next load current I_{OX} for the parameters selected in section 2.3.2. These calculated optimal trip currents reduce the circuit power loss.

2.3.2 Design Considerations

A good design of the resonant elements is important in order to reduce the peak voltage stress and the peak current stress on the devices. The converter is designed to achieve the maximum voltage gradient of 600 *V/µs* intended for low over voltage at the end of a 34m motor cable. The specifications to design the quasi resonant dc link inverter circuit parameters are as follows:

1. The inverter input voltage must be pulled down to zero for zero voltage switching (ZVS) and again boosted to the DC link source voltage.
2. The trip currents should be as small as possible in order to reduce the circuit power loss.
3. It is important to minimize the peak values of the resonant voltage and the resonant current in order to reduce the stress on circuit devices.
4. The rising and falling slope of the inverter output voltage must be low for long cable drives.
5. The resonant transition interval must be designed to be much shorter than inverter's switching frequency cycle time.

In these specifications, the specification 1 is the important condition for soft switching of an inverter. The specification 2 is satisfied with the calculation of minimum trip currents in the previous section. However, it is not possible to satisfy all other design objectives simultaneously. The proper value of the resonant components can be obtained by computer simulations.

The increase of the snubber capacitor *C* results in low *dv/dt*, but high peak resonant current i_L and resonant voltage V_{Cr}. The inductor L_r should be small so that resonant transition interval (T_S) and peak resonant voltage V_{Cr} will be small. However, a small L_r

could result in large peak resonant current of i_L and high *dv/dt*. The increase in the capacitor C_r can limit the peak resonant voltage of V_{Cr} at the cost of large peak resonant current of i_L and high *dv/dt*.

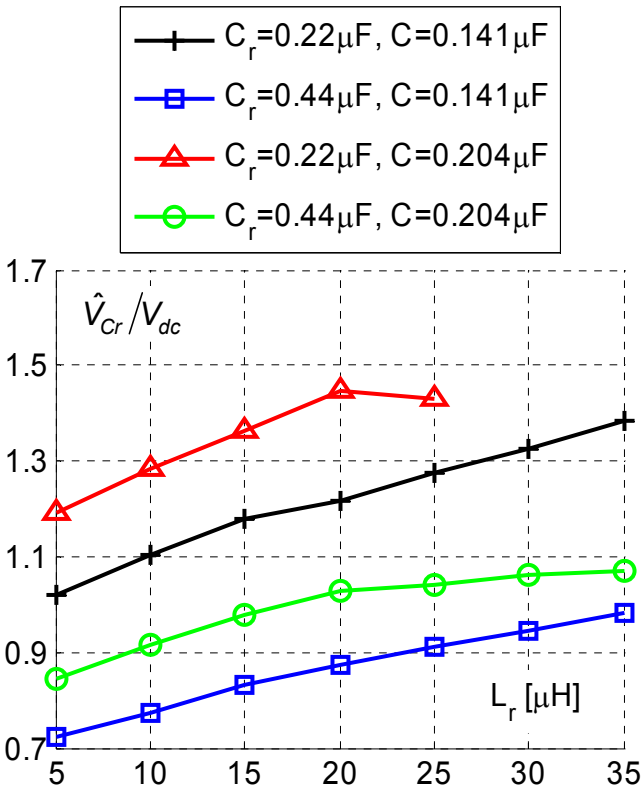


Figure 2.12 Peak values of normalized voltage (V_{Cr}) for V_{dc} = 540 V, I_O = I_{OX} = 22 A.

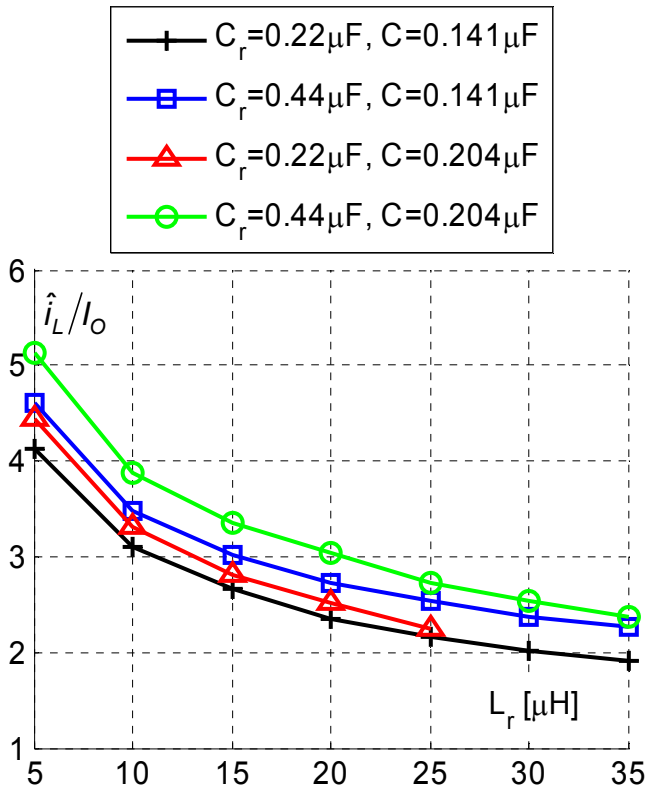


Figure 2.13 Positive peak values of normalized current (i_L) for V_{dc} = 540 V, I_O = I_{OX} = 22 A.

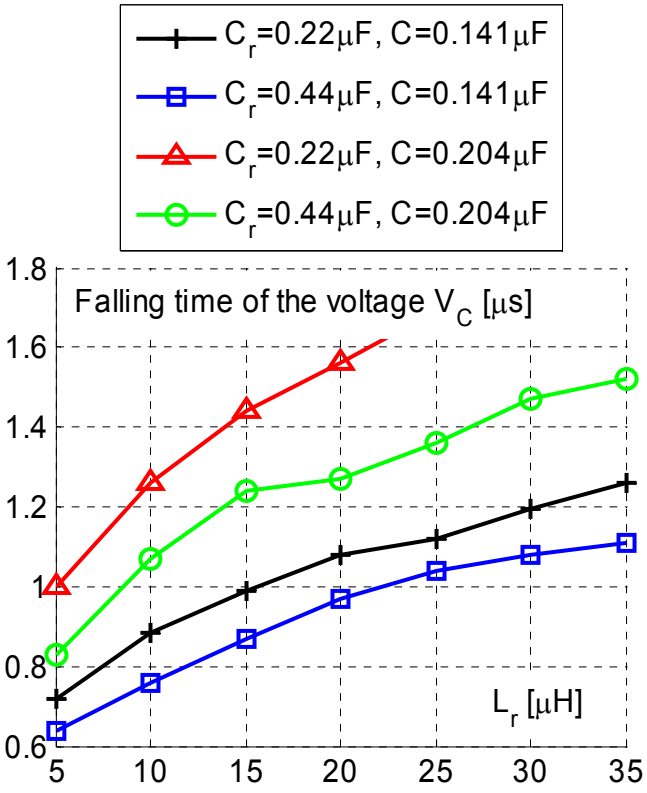


Figure 2.14 Falling times of voltage V_C for V_{dc} = 540 V, I_O = I_{OX} = 22 A.

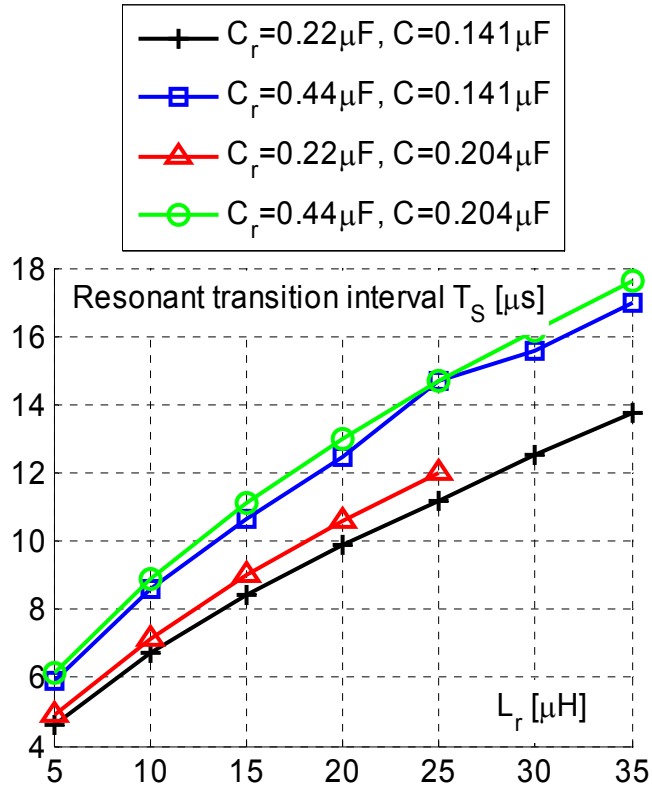


Figure 2.15 Resonant interval (T_S) time for V_{dc} = 540 V, I_O = I_{OX} = 22 A.

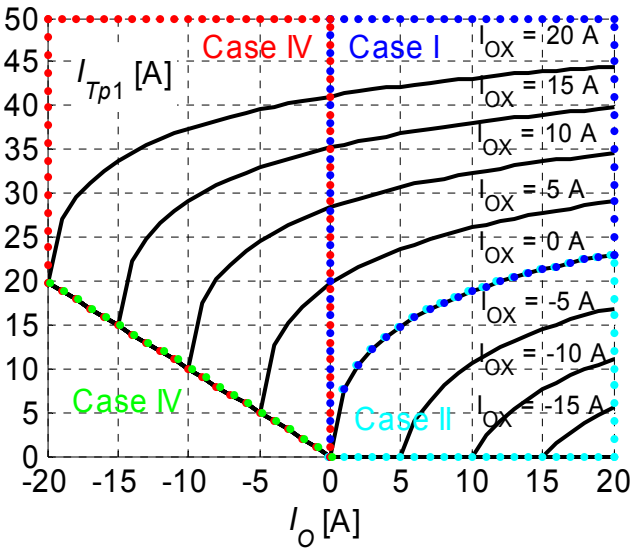


Figure 2.16 The variation in trip current I_{Tp1} according to the present load current I_O and next load current I_{OX}.

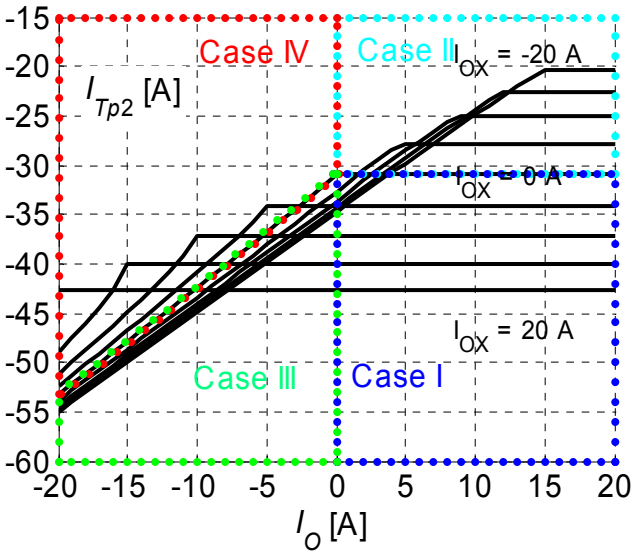


Figure 2.17 The variation in trip current I_{Tp2} according to the present load current I_O and next load current I_{OX}.

The peak resonant voltage (V_{Cr}), peak inductor current (i_L) and falling time of the voltage (V_C) are to be obtained from the equations ((2.42)-(2.69)) derived for different modes. It is difficult to obtain an analytical solution due to complex modes. A simulation model for resonant converter has been developed and implemented in Simplorer® network simulation software. The values for peak resonant voltage (V_{Cr}), peak inductor current (i_L), falling time of the voltage (V_C) and resonant transition interval (T_S) are obtained from the simulation. The simulations are done for different values of the resonant elements. The proper values of resonant components can be obtained from the simulations.

Figure 2.12 shows the variation in peak values of the normalized resonant voltage of V_{Cr} according to the inductor L_r for each value of capacitor C_r and C. Figure 2.13 shows the normalized peak current of the resonant inductor i_L for different values of the L_r, C_r and C. Figure 2.14 and Figure 2.15 show the falling time of voltage V_C and the maximum resonant interval time (T_S) respectively.

The characteristics for the parameter values variations are given above. The converter is designed to achieve the maximum voltage gradient of 600 *V/µs* and at the same to have low peak current and voltage stresses on the devices and thereby to reduce losses. The selected parameters for this resonant converter are as follows: Resonant Inductor L_r = 30 µH, Resonant Capacitor C_r = 0.47 µF and Capacitor C = 0.141 µF. The trip currents ($I_{Tp1}$and I_{Tp2}) for the selected parameters are given in Figure 2.16. These calculated optimal trip currents minimize the circuit power loss.

2.3.3 Simulation of the resonant converter

A simulation model for resonant converter has been developed and implemented in Simplorer® network simulation software. In Figure 2.18 the simulated waveforms for resonant circuit are shown. The inverter bridge switches change their status when inverter input voltage (V_C) is zero. For the selected resonant parameters, peak voltage on the resonant capacitor C_r will be always less than the DC-link voltage V_{dc}. Even though peak currents in the resonant inductor are higher, the average value of the resonant inductor current is low.

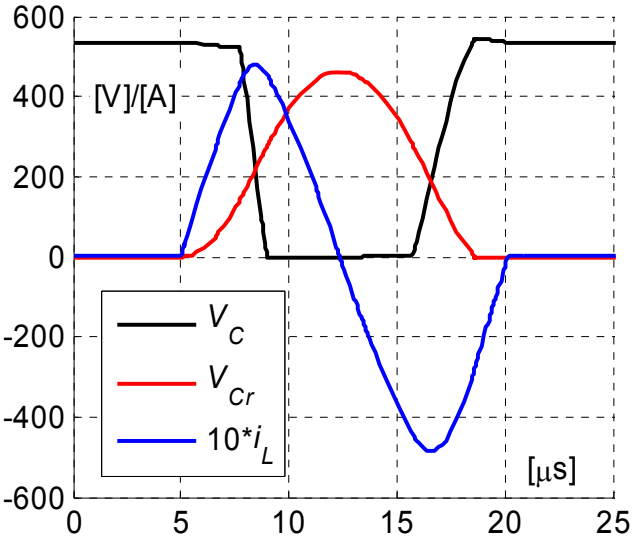


Figure 2.18 Simulated resonant circuit waveforms

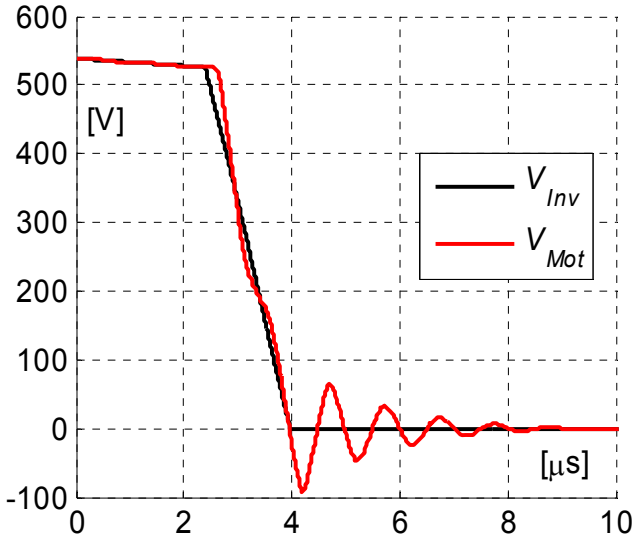


Figure 2.19 Simulated over voltage reflections

The simulation results, presented in Figure 2.19 show the effect of voltage gradient reduction, for line to line voltage, on voltage reflections at motor terminals. Here, the worst case was considered. The load current I_O has its maximum positive value. So during Mode M2, the energy stored in capacitor *C* is quickly removed, producing the fastest voltage decay for designed inverter. The resonant elements were thus designed so that, even for the worst case the overvoltage at motor terminals remains under 20% when using a 34 m, long cable, i.e. voltage slope approximately 600V/µs. Here, the long cable simulation model is taken from [76].

2.4 Motor friendly Quasi-resonant Inverter

Feeding electrical motors by long cables using PWM inverters has become lately problematic due to developments in semiconductor technology. Most used in converters, insulated gate bipolar transistors IGBTs switch voltages with high gradients, about 10kV/µs. On one hand, faster switching transients lead to the reduction of switching losses and therefore, permissible higher switching frequencies, reduction of harmonics and audible noise at motors. On the other hand, bigger voltage gradients combined with long feeders lead to HF parasitic effects, like overvoltage at motor terminals leading to insulation stress, high common mode (CM) ground current, bearing currents, etc. Many papers in a literature deal with corrective measures for aforementioned EMC effects. The most common solution in industry refers to use of filters between inverter and motor [14]-[23], with various implementations: at a motor or inverter side of the cable, for *dv/dt* reduction or for both *dv/dt* and CM voltage reduction. CM voltage can also be reduced directly with unconventional pulse-width modulation patterns [24], [27] and [28].

Resonant converters represent an alternative for hard switched converters due to reduction of switching losses. Besides this, motor-friendly characteristics can be obtained by reducing voltage overshoot at motor side cable end and CM voltage. For the switching loss reduction, *dv/dt* limitation and PWM implementation, different resonant DC-link topologies are already compared in literature [46], [47]. From these, two quasi-resonant topologies are selected and analyzed here. These two quasi-resonant DC-link converter topologies T1 and T2 are discussed in section 2.2 and section 2.3 respectively. The main advantage of topology T1 is, during mode m3, the shoot-through switching state of the inverter bridge is not needed. So the conventional 6-pack IGBT driver circuits can be used. Presence of only two passive elements (L_r and *C*) simplifies the circuit equations and

facilitates easy design of the resonant circuit parameters. The main advantage of topology T2 is the reduced power dissipation in the resonant circuit because the main inductance L_r shares the energy with the additional resonant capacitor C_r, and the circuit needs only two additional switches. On the other hand, the presence of three passive elements (L_r, C_r and C) gives rise to the complex circuit equations and causing complicated design.

The quasi-resonant DC-link inverters provide reduced voltage gradients at inverter output, during a resonant operation, as they depend on the passive elements from a resonant circuit and no longer on hard switched semiconductors. By setting the design constraints for required voltage slopes, a safe operation of motor can be obtained. In section 2.2.2 and section 2.3.2, the converters are designed to achieve the voltage gradient of 600 *V/µs* intended for low over voltage at the end of a 34m motor cable. Additional to voltage slope reduction, the common mode voltage (V_{CM}) reduction is possible by inserting a second DC-link switch S_{DC2}, as shown in Figure 2.20. The two switches S_{DC1} and S_{DC2} help in completely separating the inverter bridge from DC-link.

Extended resonant cycle: During the resonant operation, S_{DC2} is opened along with S_{DC1}. Then the dc link is completely separated from the inverter bridge and there by common mode voltage is zero during resonant operation. The zero voltage period (Mode m3/M3) during resonant operation is effectively equivalent to the zero voltage vector of PWM. In order to accommodate the zero voltage vector within a resonant cycle, the zero voltage period can be extended. Then the CM voltage during zero vector reduces to zero.

For topology T1, the zero voltage period ($t_Z = t_3 - t_2$) is controllable (Figure 2.3b) [41]. Also for topology T2, the zero voltage period ($t_Z = t_3 - t_2$) is controllable by keeping switch S_{INV} conducting. (Figure 2.10) [43]. Duration of the mode M3 can be prolonged as shown in Figure 2.21. During Mode M31, zero voltage is applied to the inverter. If we keep the switch S_{INV} closed further the capacitor voltage V_{Cr} discharges to zero and the total energy is stored in the resonant inductor only (M32). Until we open the switch S_{INV}, the inductor current i_L freewheels through the diode D_{r1} and the inverter switches (M33). In this way, the zero voltage period can be extended.

Figure 2.22 shows the simulated waveforms for an extended zero voltage period. For topology T2, the resonant capacitor voltage discharges to zero, and the total energy is stored in a resonant inductor only. In Figure 2.23, the simulated CM voltage remains at $\pm V_{dc}/6$ during PWM states ($\vec{V}_1$ and $\vec{V}_2$) and is cancelled during a resonant period, where the inverter bridge voltage drops to zero. Thus, a resonant period is used for zero vector intervals and the level of CM voltage is minimized.

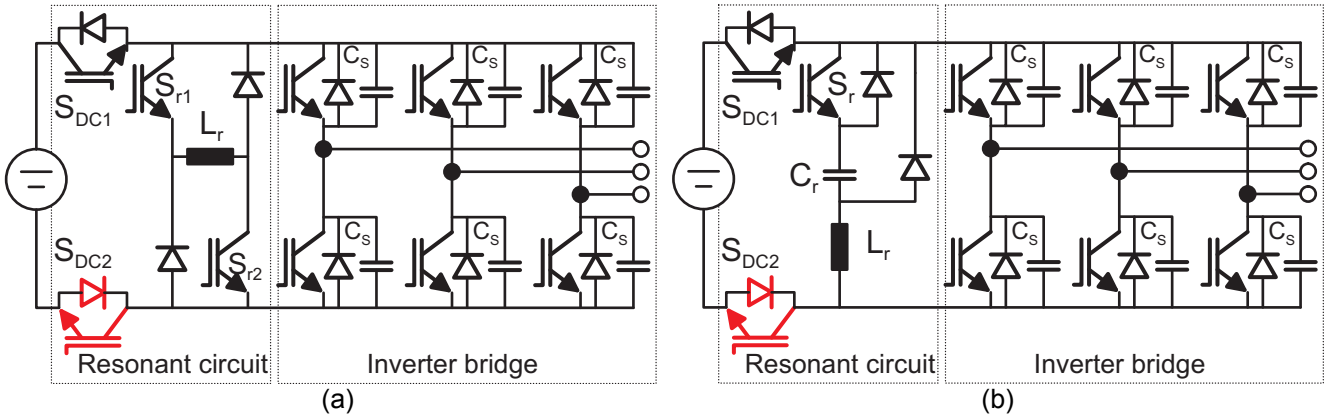


Figure 2.20 Modified circuit for common mode voltage reduction (a) T1 topology (b) T2 topology.

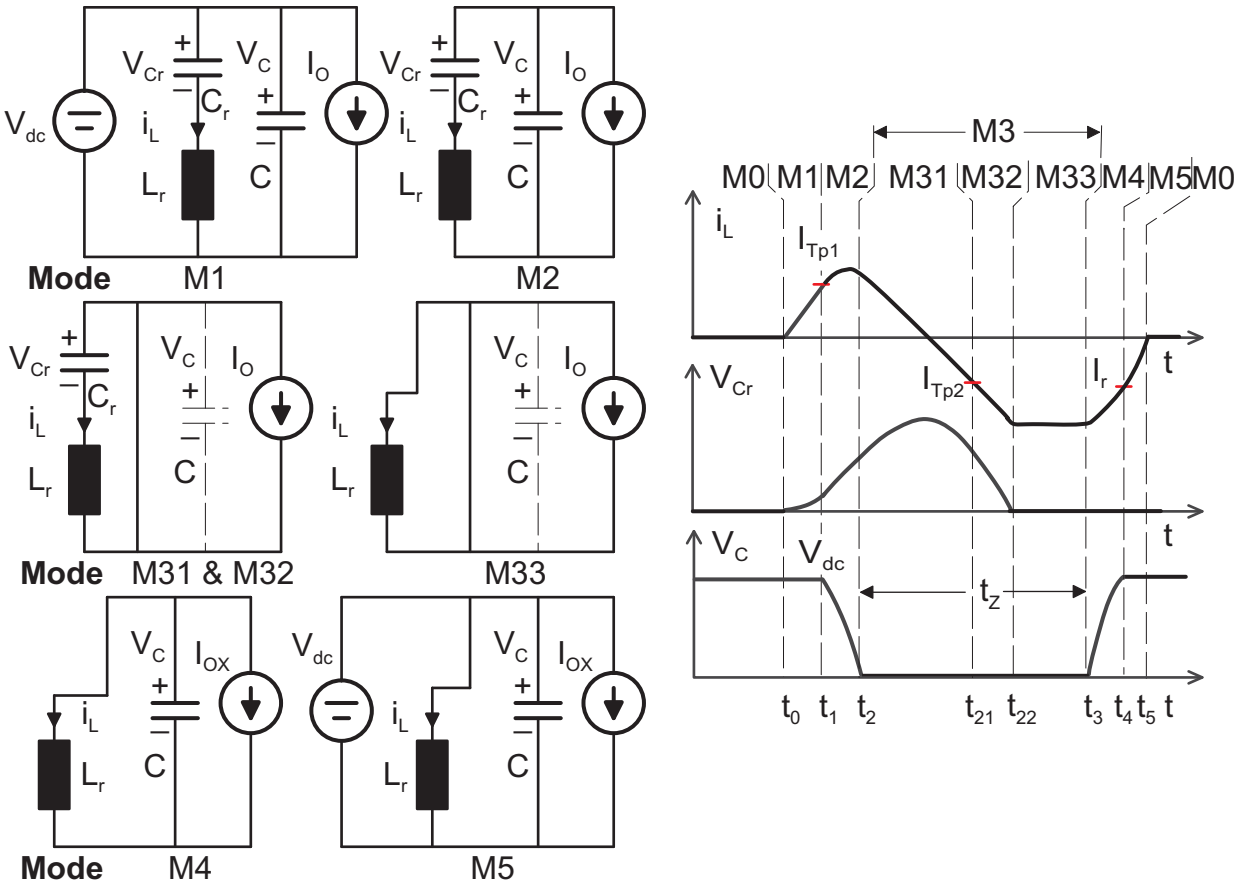


Figure 2.21 Topology T2 : Operating modes and typical waveforms for extended resonant cycle

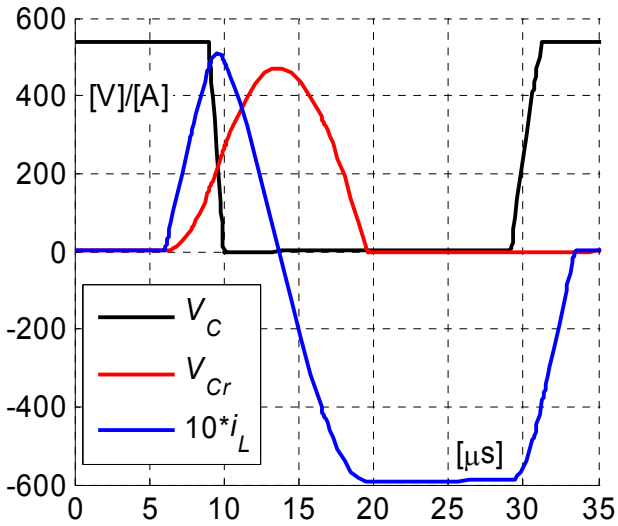


Figure 2.22 Simulated waveforms for extended zero voltage period (Topology T2)

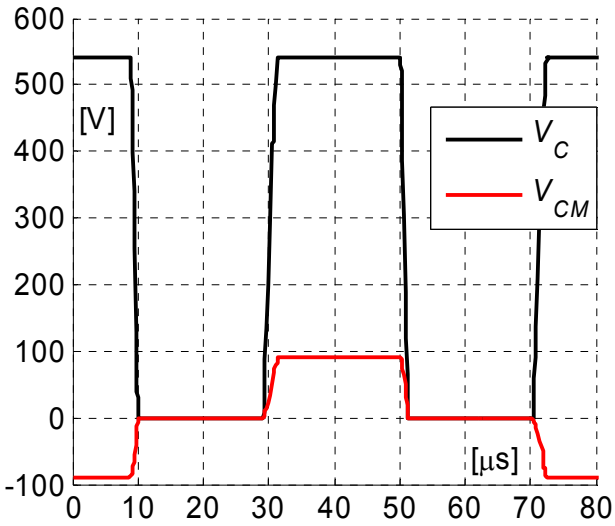


Figure 2.23 Simulated common mode (CM) voltage for modified space vector modulation

2.4.1 Modulation scheme

Conventional space vector modulation: The quasi-resonant dc link inverter changes the switching pattern under zero voltage condition. It is explicit that the resonant operation requires minimum time for current built-up, the resonant oscillation, zero voltage interval and the restoring to V_{dc}. It imposes a condition that the PWM pulse widths should be longer than the required minimum pulse duration. The converter is designed to achieve the

voltage gradient of 600*V/μs*, intended for low over voltage at the end of a 34m motor cable. Longer time is needed for resonant cycle to assure these smaller gradients. But the longer resonant cycle diminishes the active period inside a PWM period which leads to smaller possible modulation indexes. In the conventional space vector modulation, it requires 6 resonant cycles per switching period T_S, resulting in poor DC-link voltage utilization.

In a switching cycle T_s,

$$|V_{ref}|e^{j\varepsilon_{ref}}T_s = \vec{V}_0T_0 + \vec{V}_1T_1 + \vec{V}_2T_2 \tag{2.78}$$

The time T_0 is the on-time of a zero voltage vector ($\vec{V}_0$ or $\vec{V}_7$). The active vectors $\vec{V}_1$ and $\vec{V}_2$ on time durations are T_1 and T_2. During the zero voltage vector either all the upper switches ($\vec{V}_7$) or the lower switches ($\vec{V}_0$) are turned on. The QRDCL inverter produce shoot-through zero state, where all the upper and lower switches are turned on (Mode m3/M3). This zero state ($\vec{V}_{07}$) is equivalent to the normal zero voltage vector ($\vec{V}_0$ or $\vec{V}_7$), and the inverter output voltage is zero. The advantage of implementing zero voltage vector within an extended resonant cycle, i.e. $\vec{V}_0$ *and* $\vec{V}_7$ as $\vec{V}_{07}$, is the CM voltage reduces to zero. Figure 2.24 shows the conventional space vector modulation with and without using the extended resonant cycle. With an extended zero voltage period, it requires 4 resonant cycles per switching period.

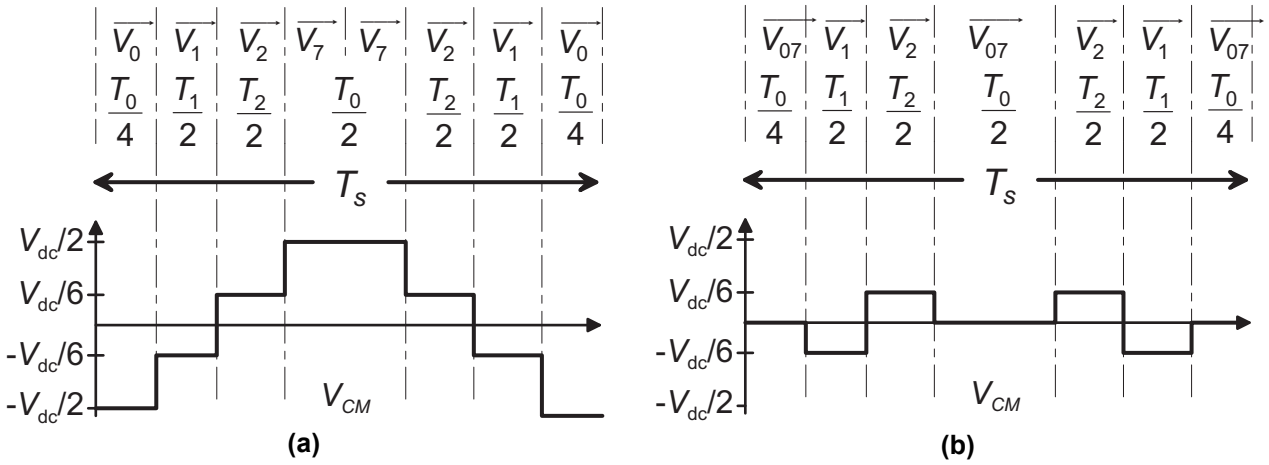


Figure 2.24 Conventional SVPWM: (a) without (b) with extended resonant cycle

<u>*Modified space vector modulation*</u>: A different modulation scheme has to be adopted so that better utilization of the DC-link is possible. Figure 2.25 shows a modified modulation where each active vector is followed by a zero vector. The extended resonant operation ($\vec{V}_{07}$) can be used in place of zero voltage vector ($\vec{V}_0$ or $\vec{V}_7$) for PWM modulation. So the modified space vector modulation requires only 2 resonant cycles per switching period T_S. The theoretical CM voltage for both modulation methods is also shown in Figure 2.24 and Figure 2.25. When using only S_{DC1}, all inverter outputs are short-circuited and connected to minus DC bus during a resonant cycle, which determines common mode voltage V_{CM} = $\pm V_{dc}$ / 2 (Figure 2.24a). By inserting an additional switch to separate also minus DC-link bus, V_{CM} is canceled (Figure 2.24b and Figure 2.25). Thus, only during PWM periods, when an active voltage vector is selected, the CM voltage will be $\pm V_{dc}$ / 6.

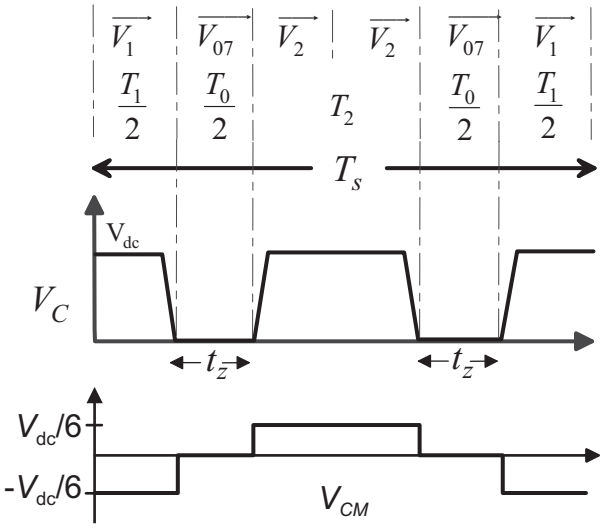


Figure 2.25 Modified SVPWM

2.4.2 Estimation of power losses

Simulation models for resonant converters are developed and implemented in Ansoft's Simplorer® network simulation software. Simulation is done with static semiconductor switches, and losses are estimated using digital signal processing blocks. Reference [49], describes the estimation of power losses from simulations using ideal switches and post processor estimation program with the help of datasheets. This method of estimation of power losses decreases the simulation time and labour effort.

The selection of semiconductor devices is discussed in section 3.2.1. First, for all the devices, the instantaneous on-state voltage ($V_{on\text{-}table}$) versus current ($i_{on\text{-}table}$) is read from the data sheets. Then the current ($i_{on\text{-}table}$) versus turn-on ($E_{on\text{-}table}$) and turn-off energy ($E_{off\text{-}table}$) are also read from the data sheets. Then the data is entered in lookup tables.

The switching moments are determined using abrupt edges on voltage and current waveforms [49]. The positive voltage edges occur at turn-off moments and the negative voltage edges occurs at turn-on moments. The turn-on voltage, $V_{on\text{-}S}$, is the first sample before the negative edge on the voltage waveform and the turn-on current, $i_{on\text{-}S}$, is the first sample after the positive edge on the current wave form. The turn-off voltage, $V_{off\text{-}S}$, is the first sample after the positive edge on the voltage waveform and the turn-off current, $i_{off\text{-}S}$, is the first sample before the negative edge on the current wave form. Based on the lookup table and given $V_{on\text{-}S}$ and $i_{on\text{-}S}$, the loss estimation program computes the turn-on energy loss ($E_{on\text{-}S}$) using a linear interpolation. Similarly, the turn-off energy loss ($E_{off\text{-}S}$) is estimated. The program computes the turn-on and turn-off energy loss using the following equations:

$$E_{on-S} = E_{on-table} \frac{V_{on-S}}{V_{on-table}} \frac{i_{on-S}}{i_{on-table}} \tag{2.79}$$

$$E_{off-S} = E_{off-table} \frac{V_{off-S}}{V_{off-table}} \frac{i_{off-S}}{i_{off-table}} \tag{2.80}$$

The on state voltages, $V_{on\text{-}C}$, are computed using lookup table and current ($i_{on\text{-}C}$) through the device. The conduction losses are averaged along an integration time T.

$$V_{on-C} = V_{on-table} \frac{i_{on-C}}{i_{on-table}} \tag{2.81}$$

The turn-on power ($P_{on\text{-}S}$), turn-off power ($P_{off\text{-}S}$) and conduction losses ($P_{on\text{-}C}$) are calculated as below:

$$P_{on-S} = \frac{1}{T}\sum E_{on-S}\ ,\ P_{off-S} = \frac{1}{T}\sum E_{off-S} \tag{2.82}$$

$$P_{on-C} = \frac{1}{T}\sum \left(V_{on-C}.I_{on-C}.\Delta T\right) \text{ where } \Delta T \text{ is the simulation step} \tag{2.83}$$

The switching losses given in the data sheets are for hard switching converter. For soft switching inverter, the switching losses are taken as approximately 10% of given losses under hard switching conditions. The switching frequency is 10 kHz.

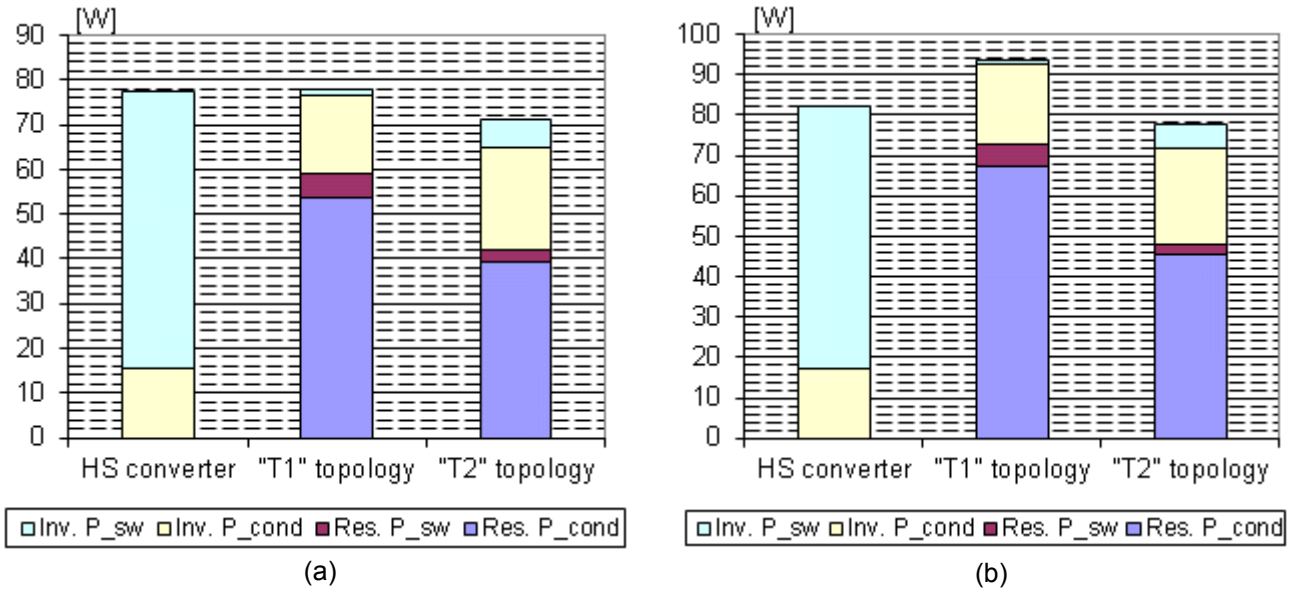


Figure 2.26 Semiconductor losses for (a) 2.8 kW motor load (b) 3.5 kW motor load

The switching and conductions losses are roughly estimated for both quasi-resonant topologies in Figure 2.20. They are compared in Figure 2.26 for two points of load operation. The converter topology T2 has low conduction and switching losses compare to T1 because of less number of resonant switches required for resonant operation. The resonant inductor losses are not included in Figure 2.26 due to a more complicated HF inductor simulation model. However, the semiconductor losses alone indicate a clear advantage for T2 topology. The resonant inductor L_r in topology T2 shares the energy during a resonant cycle with capacitor C_r. So the losses in topology T2 will be much lesser than topology T1. Therefore, this topology is chosen further for practical implementation and testing.

2.5 Conclusions

The selected quasi-resonant circuits operation principle as well as mathematical analysis and modeling are provided in this chapter. Other issues such as design considerations, design formulas are also addressed in this chapter. Simulation results are presented to confirm the design and modeling. By adding an additional switch to the resonant circuit, complete separation of the inverter bridge from DC-link is possible. This leads to an elimination of common mode voltage during the time interval of the zero voltage vectors. It is shown that motor friendly characteristics like reducing the voltage gradients at inverter output and CM voltage reduction at the motor's neutral point can be achieved by the selected two topologies. At the end, the simulations are used to estimate approximate semiconductor losses of these two topologies and the quasi resonant inverter by [43] is selected.

3 System Implementation

3.1 Introduction

In order to evaluate the motor friendly characteristics of the designed QRDCL inverter in practical case, it is very significant and necessary to further investigate the system experimentally. Therefore, a 4 kW zero voltage switching three phase inverter with induction motor load, which uses the designed resonant circuit between the DC supply and the inverter to resonant the DC-link voltage, was built in the laboratory for experimental studies. The chapter begins with the selection of semiconductor devices and passive components for the designed 4kW QRDCL inverter. In this chapter detailed description of the power electronic main circuit and control circuit are provided.

The quasi-resonant dc link inverter control is very similar to that of the conventional hard-switching inverter control except the control of a resonant circuit. The addition of a resonant circuit provides the zero-voltage switching environment for the PWM inverter. The control of the quasi resonant inverter is implemented in a FPGA. In the previous chapter, a modified space vector PWM (SVPWM) technique is adopted, to control QRDCL inverter, for better utilization of DC-link voltage. One sub section describes in detail the implementation of this modulator in FPGA. The total control of a soft switching inverter together with the motor has been realized in a single chip FPGA. In this chapter, control algorithms to implement indirect field oriented control (IFOC) in a FPGA are discussed in detail.

3.2 Power Electronic Main circuit

The quasi-resonant inverter main circuit is shown in Figure 3.1. The inverter is supplied from a 3-phase diode rectifier, and the DC-link voltage is maintained constant using large electrolytic dc-link capacitors. The DC link capacitor mainly consists of four electrolytic capacitors, i.e. two series connected and two in parallel. To perform the measurements on the hard switched semiconductor, the switches S_{DC1} and S_{DC2} are closed, and the switch S_r is open always.

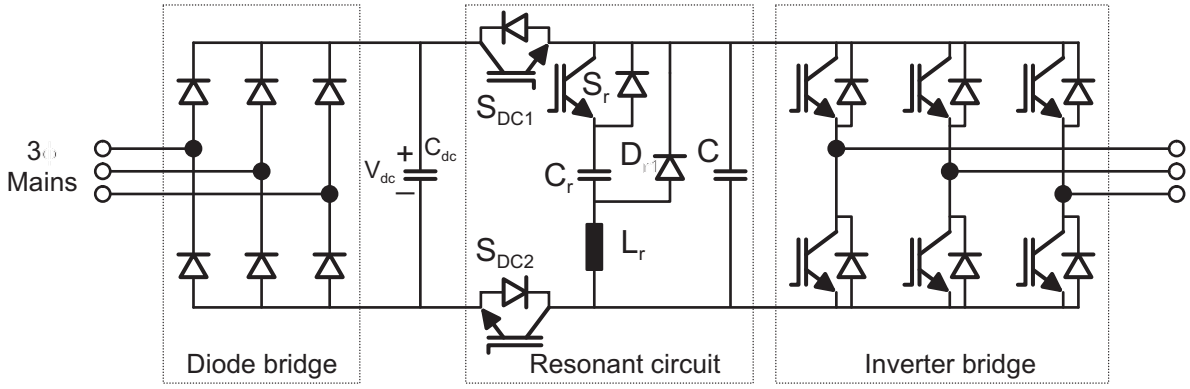


Figure 3.1 Main Circuit

3.2.1 Semiconductor devices

The research work concerning this subsection was work from the diploma thesis no: DA1347 [62]. This diploma thesis was done under both Mr. Calin Purcarea and my supervision. The part of this work is published in [84].

The selection of semiconductor devices is important for the efficiency of an entire inverter. Having ZVS condition, the switching losses are very low in inverter switches. To have low conduction losses, a new IGBT Trench - Fieldstop 4 technology is used for inverter bridge switches. The selection of resonant circuit switches is very important. The switches (S_{DC1} and S_{DC2}) inserted in series between a dc link and resonant bus, have to have very low conduction losses because they supply continuously power from DC-link to the inverter. The switches (S_{DC1}, S_{DC2} and S_r) have to operate at high switching frequency also. By using latest developments in semiconductor technology available on the market, this disadvantage can be reduced. In the future, when SiC –Fets will be commercially available for e.g. 50A switches, then these devices will be highly interesting for this application. Three semiconductor devices are compared for the resonant circuit application.

A CoolMOS Characteristics

The novel device concept of CoolMOS™ offers a new approach to overcome the drift zone resistance, which is the main source of resistivity in high voltage devices (Figure 3.2) [50]. CoolMOS™ virtually combines the low switching losses of a MOSFET with the on-state losses of an IGBT. But the breakdown voltage of the CoolMOS™ is limited to 650V. So it makes them inappropriate to be used for the switch S_r. However, CoolMOS™ can be used for DC-link separating switches S_{DC1} and S_{DC2}, where the entire DC-link voltage is shared between both the switches. Care should be taken to make both the switch share the voltage equally.

B ESBT Characteristics

The Emitter-Switching Bipolar Transistor is a combination of a NPN bipolar transistor (BJT) and MOSFET. The fast switching low voltage n-channel power MOSFET is realized inside the emitter of the BJT (Figure 3.3) [51]. The bipolar structure gives low saturation voltage, and the cascaded structure increases the device switching speed. The BJT has an enhanced voltage blocking characteristics. The ESBTs can be used for zero voltage switching applications also [55]. So the ESBTs seem to be ideal devices for the DC link switches S_{DC1} and S_{DC2}. On the other hand, ESBT needs complex driving circuits in order to get good dynamic performances.

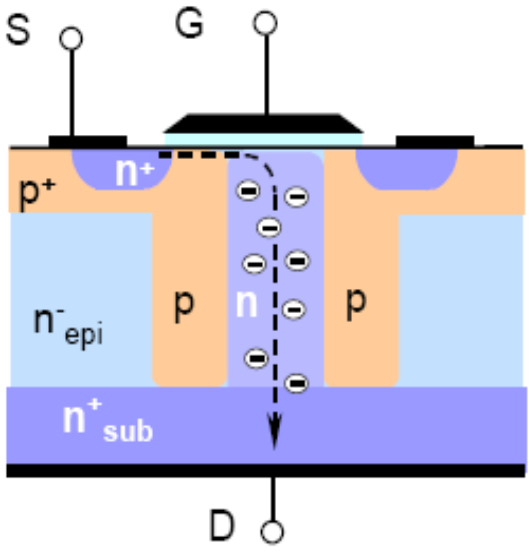


Figure 3.2 Cross section of the new CoolMOS™ high voltage power MOSFET [50]

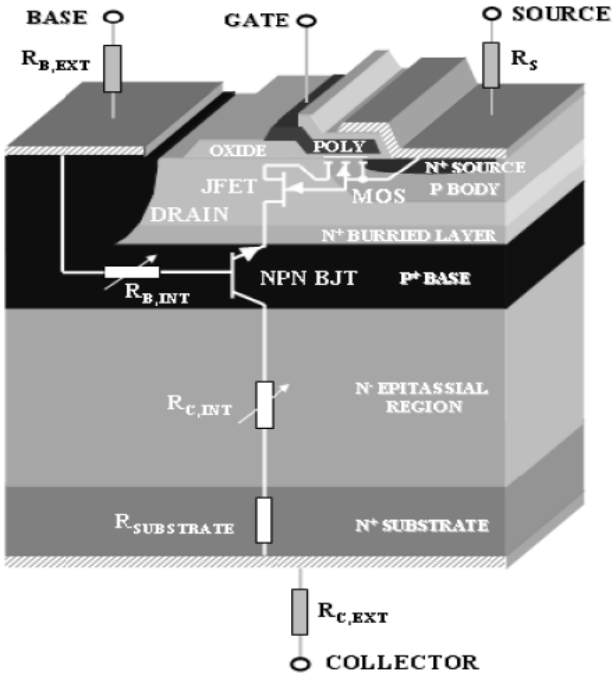


Figure 3.3 Cross section of ESBT [52]

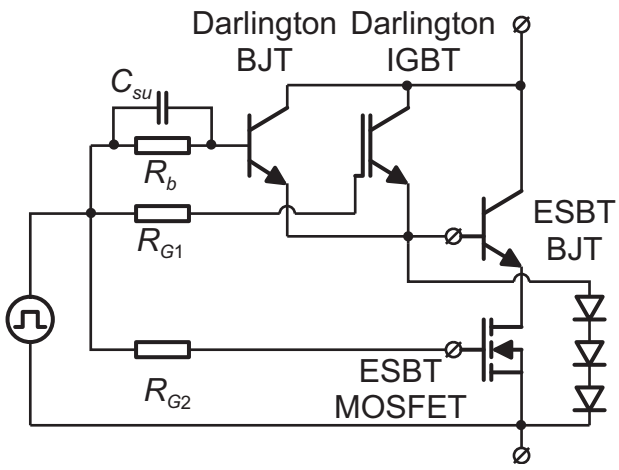


Figure 3.4 Darlington driver

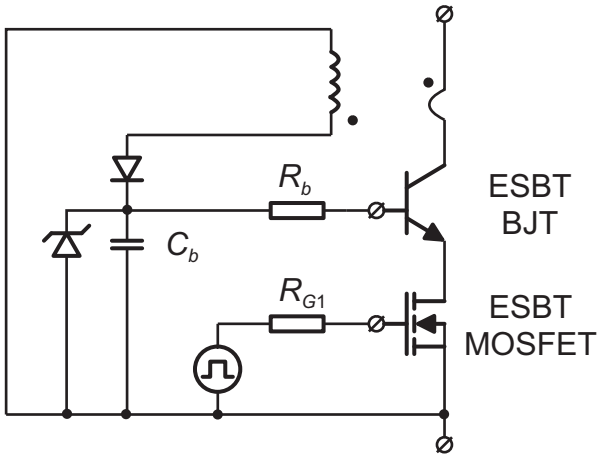


Figure 3.5 Proportional driver

In order to drive the BJT and MOSFET independently two separate terminals, gate and base, are required. Thus four terminals are necessary for the cascaded structure. A standard PWM driver can be used to drive the gate of the ESBT, whereas a special driver is needed to feed the base of the ESBT. Two driving circuits presented in Figure 3.4 and Figure 3.5 are tested. In Figure 3.4, the Darlington connection of BJT in parallel with IGBT produces the required base current [52]. High base peak current at turn-on will be quickly injected by the Darlington IGBT, and later the base current is controlled by the Darlington BJT saturation level which in turn depends upon the load current. At high load currents, if the Darlington BJT is out of the saturation, both BJT and IGBT together supply the base current. Due to that, the forward voltage drop across the IGBT increases, and thereby causing increased losses in ESBT at high load currents. The experimental results show that the ESBT turn-off is delayed under ZVS conditions.

The next driving circuit is the proportional driving schematic discussed in [52] and is shown in Figure 3.5. Here, the base current is dependent upon the load current and the fastest turn on is possible by the base capacitance C_b. But at high load current, the parasitic effect due to the core is substantial and producing the losses. The drawback of such a driver is the need to discharge the magnetization current stored inside the transformer's core, which makes it difficult to implement for S_{DC1}. On state of this switch is much longer than off state, and therefore, additional demagnetization paths have to be provided. Under ZVS condition, the capacitance C_b is discharging over the base-collector diode of BJT. Even though ESBTs have high breakdown voltage and low conduction losses, these devices need complex drivers and maintain switch closed is difficult under ZVS condition. In conclusion, the ESBT switch needs a complex driver and was found to be inappropriate for this application [62].

C IGBT Characteristics

IGBT fourth generation devices are the combination of both the field stop and the trench gate technology [56]. The IGBT4 along with the EmCon4 Diode is optimized for reduced conduction losses, switching losses and higher softness characteristic compare to its corresponding predecessor the IGBT3-T3. Still, IGBT trench-FS 4 possess large turn-off delay due to Trench gate technology. However, this IGBT can be used for the resonant switch S_r, since the turn-off delay is not critical for this switch. The switch S_r can be turned-off from at any time instant between the resonant current is crossing zero to the end of the mode M3.

All three semiconductor devices are compared in [62] for resonant circuit application. At the end, for DC-link separating switches S_{DC1} and S_{DC2}, CoolMOS™ devices are selected. For resonant switch S_r, IGBT4 is selected.

3.2.2 Resonant elements

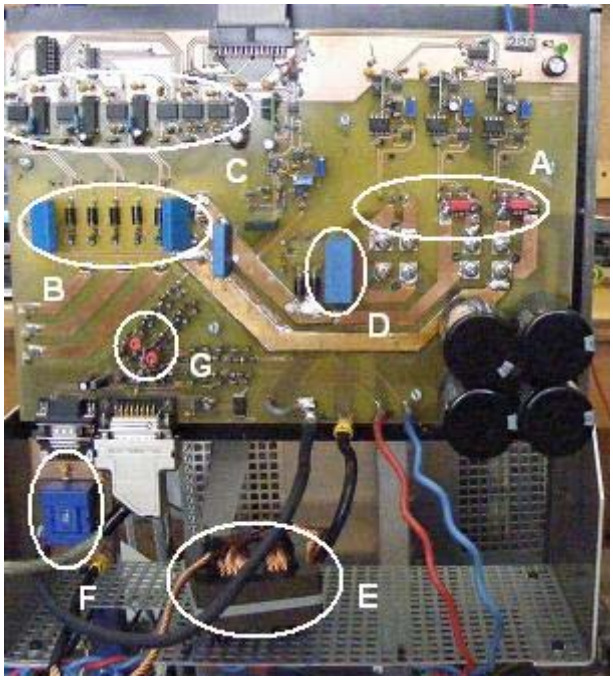
The circuit has three passive components to be selected, L_r, C_r and C, see Figure 3.1. The design expressions for this circuit are determined in section 2.3.2. The passive component values for the selected quasi-resonant topology are L_r = 30 µH, C_r = 0.47 µF, and C = 0.141 µF.

The capacitor C consists of three 0.047 µF discrete capacitors connected in parallel to give a total capacitance of 0.141 µF. The converter should also be operated under hard switching conditions. It is advantageous to distribute the capacitance among the IGBT modules, since they serve as over voltage snubbers in hard switched case [45]. The capacitor C and resonant capacitor C_r used are consisting of metallized polypropylene (MKP) film capacitors.

The specification for the resonant inductor design is given in Table 3.1. Magnetic core is used to avoid interference with near-by components. A magnetic core with high saturation flux density is necessary to avoid the inductor's saturation at resonant peak currents. The selected ferrite core (3C90)'s saturation density is 0.38 T at 100°C, 10 kHz [65]. Introducing an air gap will reduce the slope of the B-H curve. The design procedure of the inductor is discussed in Appendix A. The inductor was designed to be wound with Litz wire to avoid skin effect [2]. Litz wires are used in order to reduce the eddy currents at high frequencies. By avoiding to wind in the middle, eddy current losses in the presence of an air gap can be reduced [64].

Table 3.1: Resonant inductor specification

Core	*Size*	A_L (nH)	*N*	A_{cu} (mm^2)
3C90	E65/32/27	250	11	10



- A : Resonant circuit switches
- B : 6-pack Inverter bridge
- C : Individual drivers
- D : Resonant capacitor
- E : Resonant inductor
- F : Inductor current sensing board
- G : DC link full voltage and zero voltage detection

Figure 3.6 Inverter board

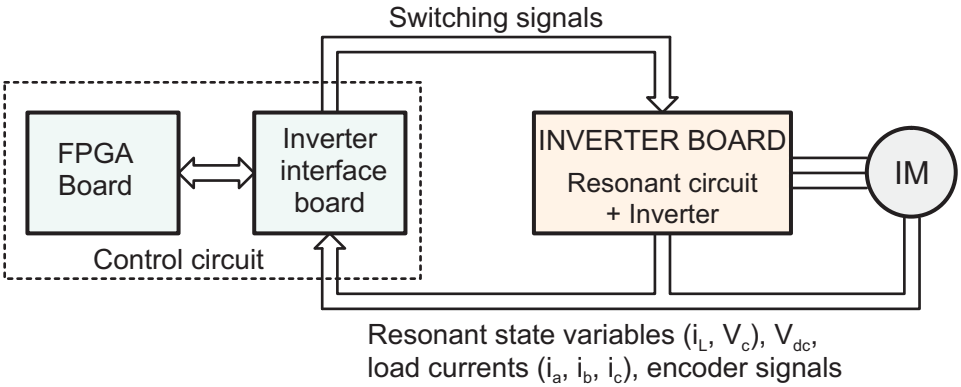


Figure 3.7 Control scheme

3.2.3 Design of inverter board

The research work concerning this subsection was work from the diploma thesis no: DA1347 [62]. This diploma thesis was done under both Mr. Calin Purcarea and my supervision.

Figure 3.6 shows the inverter board. The three-phase inverter bridge and resonant circuit switches are mounted on a heat sink. During mode M3, all the inverter bridge switches are turned on simultaneously. So a shoot-through state of the inverter bridge is necessary. The available 6-pack drives will not allow the shoot-through state of an inverter. So, individual drivers are used for the inverter bridge and also for resonant circuit switches. The snubber capacitor *C* is distributed near to the inverter bridge. The resonant inductor L_r is placed outside of the board. So that different inductor cores can be tested for the same application. During the freewheeling mode of the inductor current, the negative peak current i_L freewheels through the inductor, diode and inverter bridge switches. The width and thickness of a PCB path carrying this peak current should be large enough to avoid melting.

3.3 Control circuit

In this section, the QRDCL control circuit is described. The controller is used to control the resonant circuit, inverter and motor. Each switching operation must be preceded by an auxiliary resonant circuit operation. The quasi-resonant operation is conditioned by triggering thresholds of the inductor current and capacitor voltage. One resonant cycle takes a minimum of 16 µs time interval, where two trip current levels must be compared with references. In the same time interval, switching signals for three resonant switches and six inverter switches must be sent to the drivers. Due to short resonant cycle and fast control decisions involved, a fast controller like FPGA (Field Programmable Gate Array) is needed for controlling resonant circuit elements.

The control program is implemented in a FPGA, and the switching signals are transferred to the inverter through an interface board (Figure 3.7). The FPGA board together with the inverter interface board is aimed at generalized motor control and is equipped with required analog and digital interfaces.

3.3.1 FPGA (Field Programmable Gate Array)

In the literature, FPGA implementation is mostly limited to space vector modulation of power converters [66]-[68]. For the control of ac drive, a FPGA in combination with DSP or PC is used. FPGA has a capability of executing several processes in parallel. So the speed of a FPGA is much higher than DSP and microprocessor.

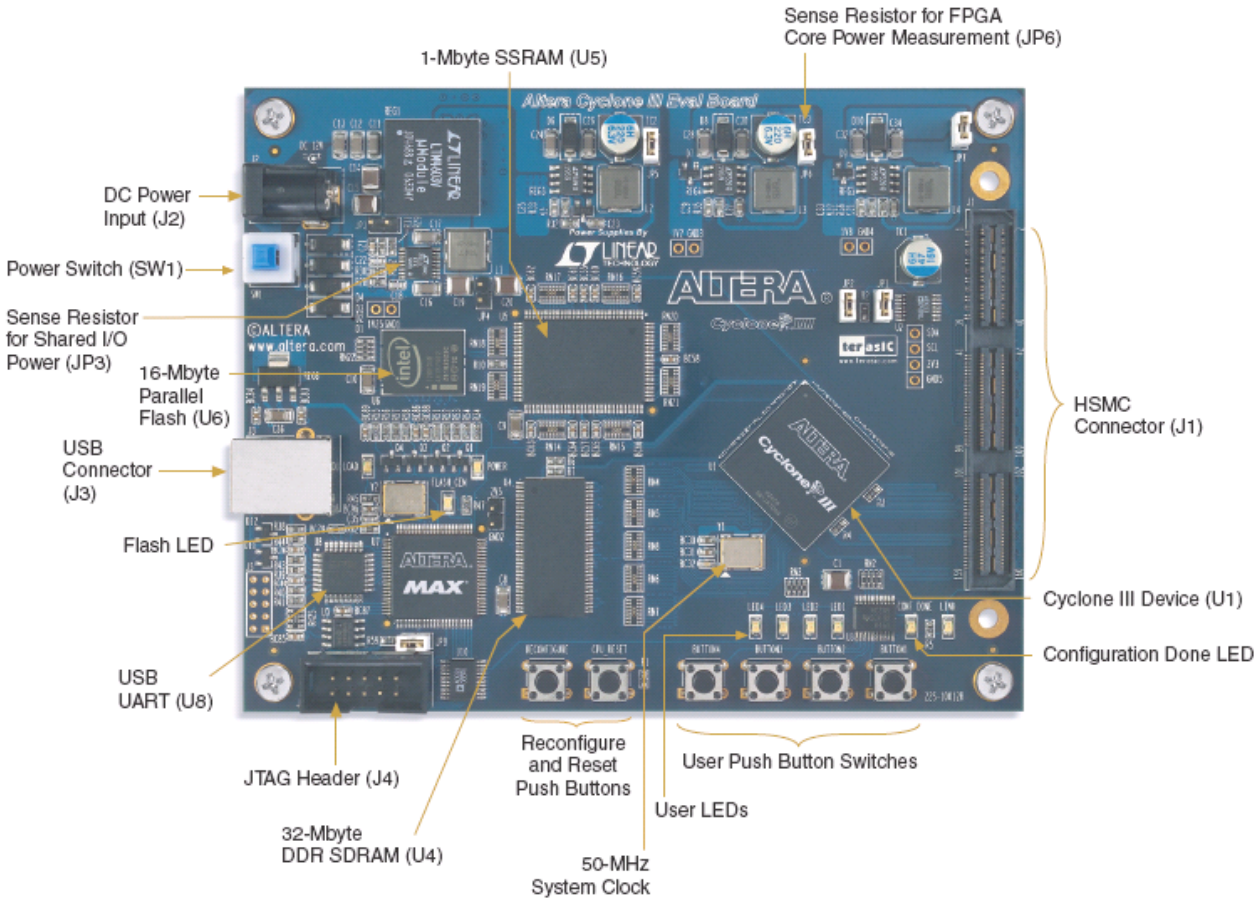


Figure 3.8 Cyclone III FPGA starter board layout and components [72].

The recent advances in FPGA technology offer us the bigger size, higher speed and large number of I/Os for lower price [69]. So, the total control of the inverter together with the motor can be implemented in a single chip FPGA. It reduces the total hardware count and provides a low-cost solution.

A special attention must be paid when choosing the size of a FPGA unit. It must contain sufficient logic cells to implement both resonant cycle control and induction motor control. A FPGA unit from Altera®, Cyclone III® family with 25k cells, was chosen [70]. It is included in Cyclone III FPGA starter kit along with additional memory blocks of SSRAM (1MB) and DDR SDRAM (32MB) [72]. These memory blocks are used to store the trip currents and the application data. Altera's Quartus II programmer software is used for programming the FPGA. An USB interface to the Cyclone III device facilitates for external FPGA configuration and communication with applications running on the FPGA. Figure 3.8 shows the selected cyclone III FPGA starter board for control implementation.

3.3.2 Design of interface board

The communication between FPGA and quasi resonant inverter is realized with the help of an interface. The main tasks of this interface board (Figure 3.9) are

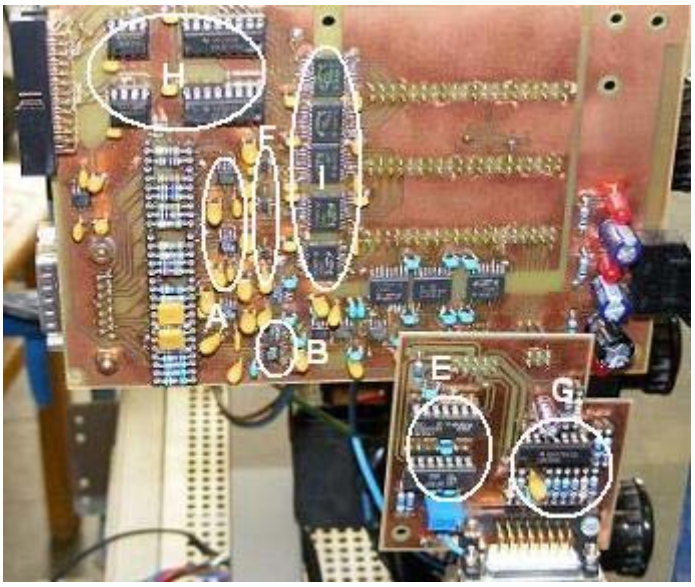
- Acquisition of resonant inductor current (i_L), snubber capacitor voltage (V_C) and DC link voltage (V_{dc}).
- Comparison of the resonant inductor current (i_L) with the trip current values (I_{Tp1} or I_{Tp2})
- DC link full voltage sensing circuit

- Inverter bridge input voltage (V_C) zero crossing detection
- Protection for resonant circuit over current
- A/D conversion of the load currents for both resonant circuit and motor control.
- Encoder interface
- Transmission of switching signals to gate drivers
- Isolators

A Acquisition of resonant state variables (i_L and V_C) and DC-link voltage (V_{dc})

The resonant inductor current i_L is measured with a LEM current transducer of type LAX 100–NP, which has a rated current of 100 A. The main advantages gained by using LEM transducer are galvanic isolation and high bandwidth. The galvanic isolation is important between the high-voltage power circuit and low-power control circuit. A high bandwidth of current measurement is not necessary since the measured current is compared only against a pre-set value (I_{Tp1} or I_{Tp2}). But anyways the current measurement is necessary, so the high bandwidth current transducer is used. The current measurement is implemented near to the main power circuit and the current output is transferred to the interface board via DB15 connector. A burden resistor on the interface board converts it to the voltage. The output voltage is differential and will be in the range of ±5V for ±100A input current. With the help of the AD8066 amplifier, the output is converted to a single ended and positive output (0 to 10V). It is necessary because the output of the digital to analog converter (DAC), which generates analog trip currents, is from 0 to 10V.

The resonant cycle is completed when the inverter bridge input voltage V_C reaches the DC link voltage V_{dc}. Both the voltages (V_C and V_{dc}) are measured by typical precision voltage divider circuits and are compared against a comparator. A voltage divider reduces the maximum voltage that can be measured across the device to levels that are safe to the comparators. The levels of the measuring voltages are not sensitive to the noise. So a simple voltage divider circuit is sufficient to measure them. A high bandwidth measurement or any complicated circuit is not necessary. The voltage divider circuits are implemented on the power circuit board, and the reduced low level signals are transferred to the interface board via DB15 connector. The differential signals are transferred to single ended signals using an AD8066 amplifier.



- A : Amplifiers
- B : Trip current level detection
- E : Resonant inductor over current measurement
- F : A/D converters
- G : Encoder interface
- H : Differential line drivers
- I : Isolators

Figure 3.9 Inverter interface board

B Trip current level I_{Tp1} and Trip current level I_{Tp2}

The energy stored in the resonant elements L_r and C_r ensures that the capacitor voltage V_C can able to return to DC-link voltage at the end of the resonant cycle. The energy storage interval is finished when the inductor current i_L reaches the trip current I_{Tp1}. It requires the sensing of the current i_L continuously. This current could be converted to a digital value using an ADC and compared with the trip current I_{Tp1} in FPGA. Slow sampling ADC results in storing more energy in the resonant elements than required. Fast converting and high resolution ADC is expensive. The proposed way is to convert the trip current level I_{Tp1} to analog value using DAC and compare the analog signals, as shown in Figure 3.10. The trip current is calculated beforehand and given to the DAC. So, high speed DAC is not required.

Initially, the trip current I_{Tp1} is given to the DAC input. When the inductor current reaches the first trip current, the second trip current I_{Tp2} is given to the same DAC, as shown in Figure 3.10. The 16-bit AD5543 DAC is used. The output of the DAC is unipolar ranging from 0 to 10 V, which corresponds to ±100 A.

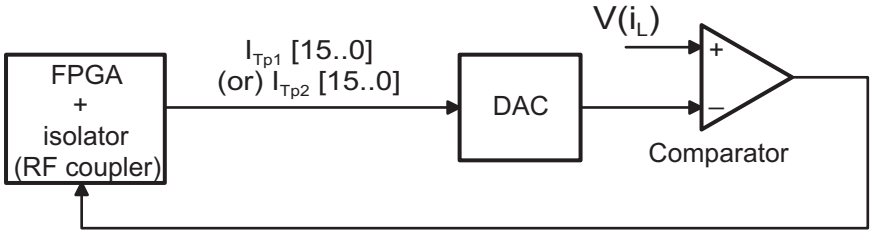


Figure 3.10 Comparison of resonant inductor current against trip currents

C DC link Full Voltage Sensing Circuit

Once the inverter bridge input voltage V_C returns back to the DC-link voltage V_{dc}, the switches S_{DC1} and S_{DC2} are turned-on, there by connecting the DC-link again to the inverter bridge. As discussed before, both the voltages are measured by typical precision voltage divider circuits and compared using a comparator (Figure 3.11). The voltage divider circuits are implemented on the power circuit board, and the reduced low level signals are transferred to the interface board and there compared with a LT1719 comparator.

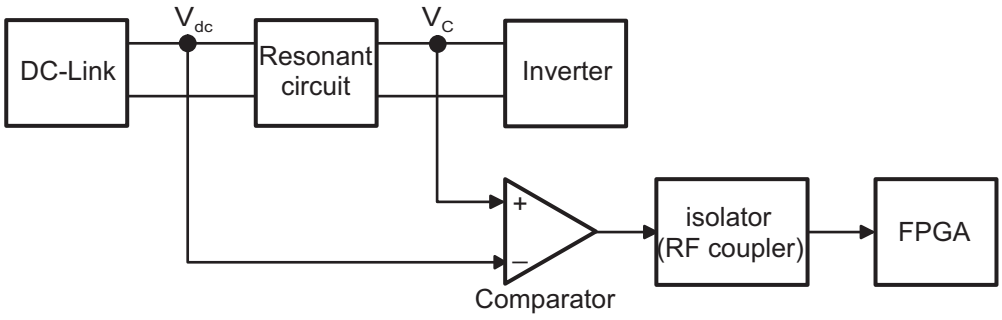


Figure 3.11 DC link full voltage sensing circuit

D Inverter bridge input voltage zero crossing detection

In order to switch the inverter power devices at zero voltages, the inverter bridge input voltage (V_C) zero crossing point must be detected accurately. This is accomplished by using zero-voltage crossing detector circuit given in Figure 3.12 [73]. Once the voltage in the soft switching device falls/drops below Vg, the MOSFET turns-on. Then, the voltage across the load resistance (R_O) is substantially equal to the voltage across the inverter

bridge V_C. The source of the MOSFET is coupled to a comparator circuit for comparing the voltage across the load resistance to a zero voltage reference. This circuit enables accurate and reliable detection of the zero-voltage crossing, when compared to a typical precision voltage divider and comparator circuit. This circuit is implemented on the power circuit, and the comparator output voltage is transferred to the interface board via communication cable.

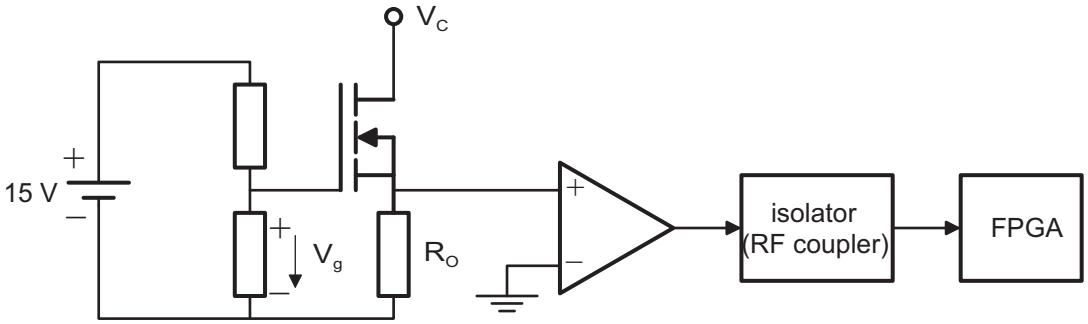


Figure 3.12 Inverter bridge input voltage zero crossing detection

E Protection for resonant circuit over current

In case of a failure of a diode D_{r1}, a short circuit may result in the resonant circuit which saturates the inductor. The resonant circuit should be protected against over current. The inductor current is compared with a reference value, which is the allowed maximum inductor current. If the current i_L crosses the ± i_{Lmax}, then an error signal is reported to the FPGA (Figure 3.13).

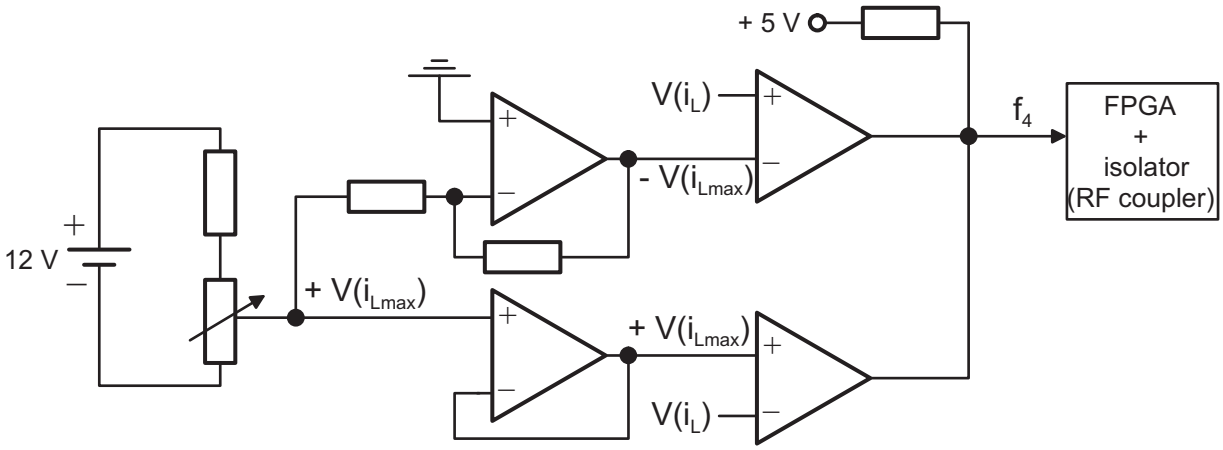


Figure 3.13 Protection for resonant circuit over current

F A/D conversion of the load currents

The current detection is realized through CMS 2025 magnetoresistive current sensors (Figure 3.14, Figure 3.15). The three analogue current signals (i_a, i_b, i_c) are routed to the inputs of three 12-bit serial analog-to-digital converters (ADS 7876). The outputs of the analog-to-digital converters are brought to the FPGA. All the currents are sampled at the same time. So the control signal pins (/CS, SCLK) of all three ADCs are connected together in the layout. FPGA generates control signals. The sampling rate of the analog-to-digital converters is set to 2 µs. FPGA is capable of parallel processing. So expensive, high speed parallel ADCs are not required and also the reduced number of pins simplifies the interface board circuit layout. Filtering of the current signals and over current protection is implemented in FPGA.

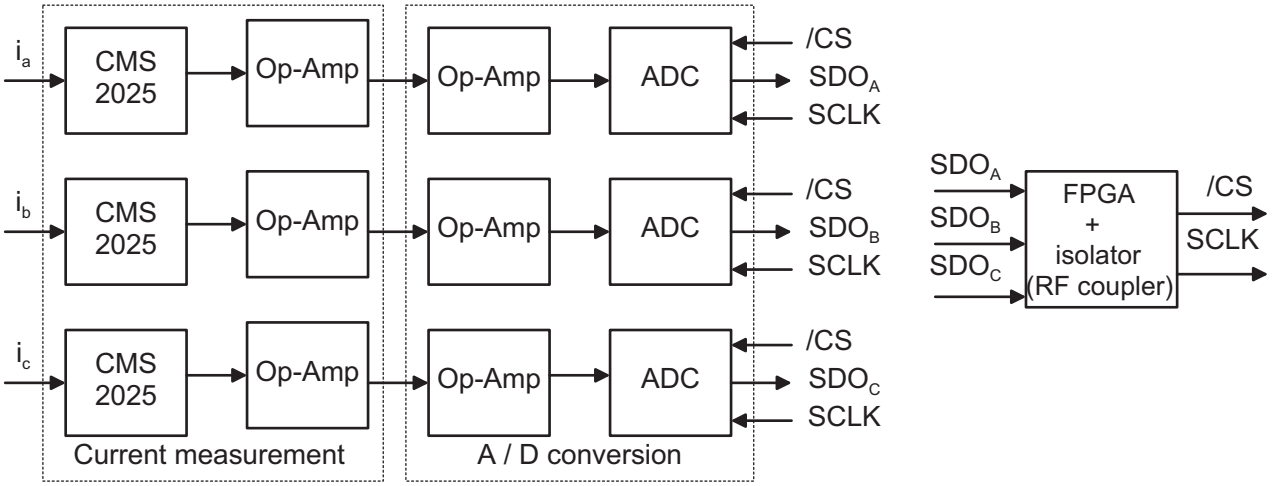


Figure 3.14 Current measurement and A/D conversion of load currents

Figure 3.15 Current measurement board

G Encoder interface

A rotary encoder ROD 486 from Heidenhain Company is mounted to the shaft of the motor. This encoder provides two sinusoidal incremental signals phase shifted by 90° (el.) and a reference mark signal. The analogue sine and cosine signals (with 5000 periods per turn) provided by the encoder are differential and have a magnitude of 1V peak-to-peak. The signs of the incremental signals are determined using hysteresis comparators (Figure 3.16). The hysteresis voltage is nearly 50 mV for 5 V output. The outputs of the comparators are brought to the FPGA.

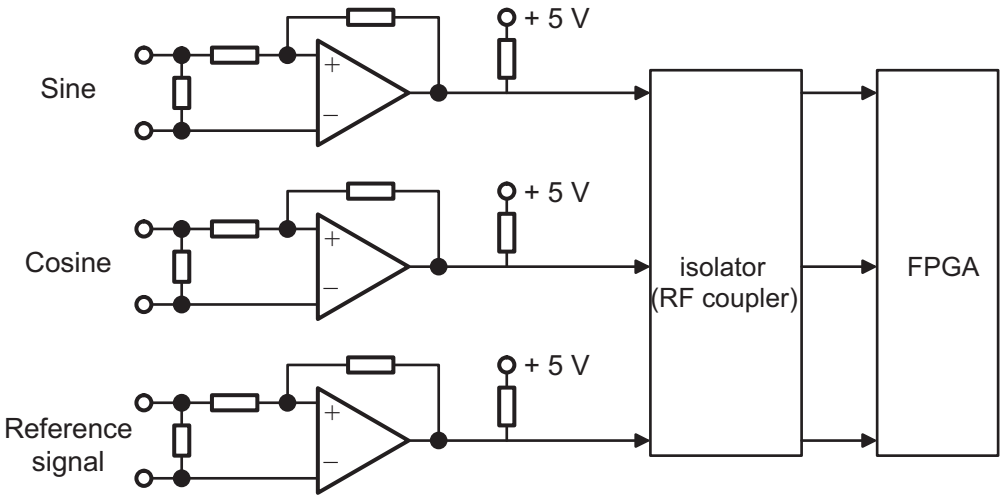


Figure 3.16 Encoder interface

H Transmission of switching signals to gate drivers

The inverter bus connects the FPGA interface board with an inverter board. It has 12 parallel signals implementing the RS 485 differential signaling standard. Out of these

12 signals, 9 signals are switching signals to the quasi resonant inverter. Two signals are desaturation detection output and zero voltage detection output from the inverter.

I Isolators

The signals from and to the FPGA are isolated by using Silicon labs Si8440 isolators. These isolators provide isolation (2500 V_{RMS}), high speed operation (150 Mbps) and level shifting of voltage (5V ↔ 2.5V) also. The selected FPGA starter board pins I/O standard is 2.5 V. In order to communicate with the interface board voltage level shifting is necessary. Even though, these isolators are expensive, the combined functions make the design of the interface board simple.

3.4 Control Software

Altera's QUARTUS II ® web edition FPGA design software is used to implement the control of the inverter and the induction motor. The field oriented control method is widely used for induction motor drives. Researchers at Siemens and Darmstadt University of Technology (Jötten, Hasse) developed the theory of field-oriented control in 1968-1969. The decoupled control of torque and flux in an AC motor has come to be known as a field oriented control. With this control, the motor can provide a good dynamic response as that obtained from DC motor drives. At the beginning, this method could not be readily applied because of the complex signal processing. With the progress of microelectronics, it is no longer a serious constraint and field oriented control AC drives emerged as better alternative to DC motor drives in high-performance applications [3], [6].

The implementation of this control scheme in a FPGA is discussed in this section. An essential feature that is necessary to implement the indirect field orient control (IFOC) in a FPGA is the capability to perform multiplications and divisions. QUARTUS II has basic block functions for multiplications and divisions of integer numbers. By using the normalized variables, the need for the floating point operations is avoided. The control is written in a very simple Altera Hardware Description Language (AHDL). The overall design is downloaded to the Cyclone III FPGA starter kit using USB connection.

The indirect field oriented controlled induction machine is fed by the quasi-resonant DC-link soft switching inverter. The total control of a soft switching inverter together with the motor has been realized in a single chip FPGA. The control algorithm has decomposed into several blocks. All the blocks execute in parallel with individual sampling rates. By using a state machine, each of these individual blocks can be forced to execute sequentially, thereby having the advantages of both sequential and parallel processing.

The firmware in the FPGA can be divided into sixteen major functional blocks and is shown in Figure 3.17.

1. ADC control – Controls the three analog to digital converters.
2. Encoder counter control – counts the periods (coarse position) based on the sign of incremental signals.
3. Speed calculation – The differentiation is implemented together with the low-pass filter of first order, which computes the speed signal from the position.
4. Speed reference value filter – It is a first order low pass filter with the time constant of speed control.
5. Speed controller – a PI controller with anti-windup is used.
6. Currents abc to αβ transformation – Clarke transformation is used.
7. Currents αβ to dq transformation – Park transformation is used.
8. Current (i_d) controller – a PI controller with anti-windup is used.
9. Current (i_q) controller – Identical to the current (i_d) controller.
10. Voltages dq to αβ transformation – Park transformation is used.

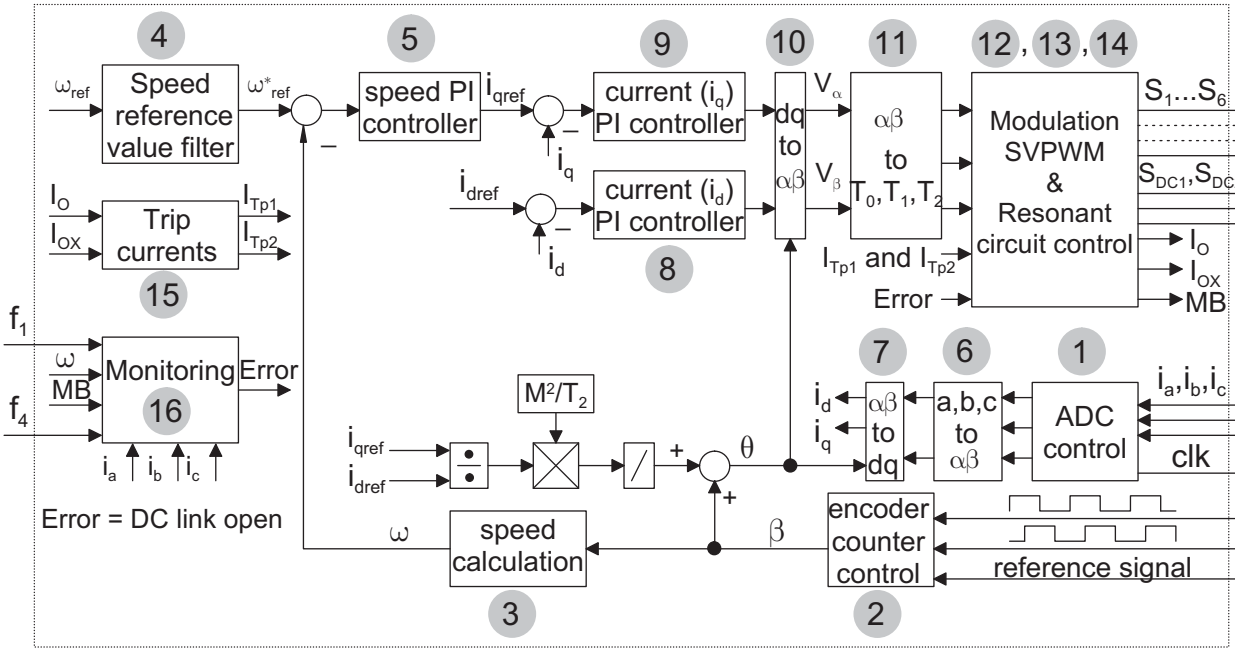


Figure 3.17 Block diagram of indirect field oriented control and quasi resonant DC-link inverter control in a FPGA

11. Calculate switching times – Based on space vector PWM, switching times are calculated.
12. Calculation of modified switching times – For a resonant cycle implementation, short vector on times are eliminated.
13. Modulation scheme – The switching times are compared against a triangular carrier and switching instants are generated.
14. Control of a resonant circuit and inverter bridge – Every change in the inverter switching status is done during a resonant cycle zero voltage interval.
15. Trip currents look up table – Based on the inverter input currents, trip currents are recalled from the SSRAM memory.
16. Monitoring – This block monitors the signals and in case of fault, disconnects the DC link capacitor from the inverter bridge.

3.4.1 ADC Control

Analog to digital converter (ADC) control has a 2 µs conversion timer. When a `*Start*´ signal is asserted, the ADC control state machine immediately asserts the chip select signal (*/CS*). With the falling edge of */CS*, the input signal is sampled, and the conversion process is initiated (ADC: ADS7886). The device (ADC) outputs the data while conversion is in progress.

The control signals are common to all three analog to digital converters. The three serial data outputs (SDO_A, SDO_B and SDO_C) from ADC´s are available to the FPGA on the falling edge of the *SCLK*. FPGA is programmed to read the data only when *SCLK* is high. The state machine is shown in Figure 3.18. The data bits (SDO_A, SDO_B and SDO_C) are stored in temporary registers TMP-I_A (12-bit), TMP-I_B (12-bit) and TMP-I_C (12-bit). The conversion ends on 16th falling edge of *SCLK*. The 12-bit data is available after a maximum time of 1.28 µs. After that, ADC control state machine updates the content of registers I_A (12 bit), I_B (12 bit) and I_C (12 bit). When the conversion timer hits 2 µs, a new conversion is started, and after it is finished, new values of currents will be available.

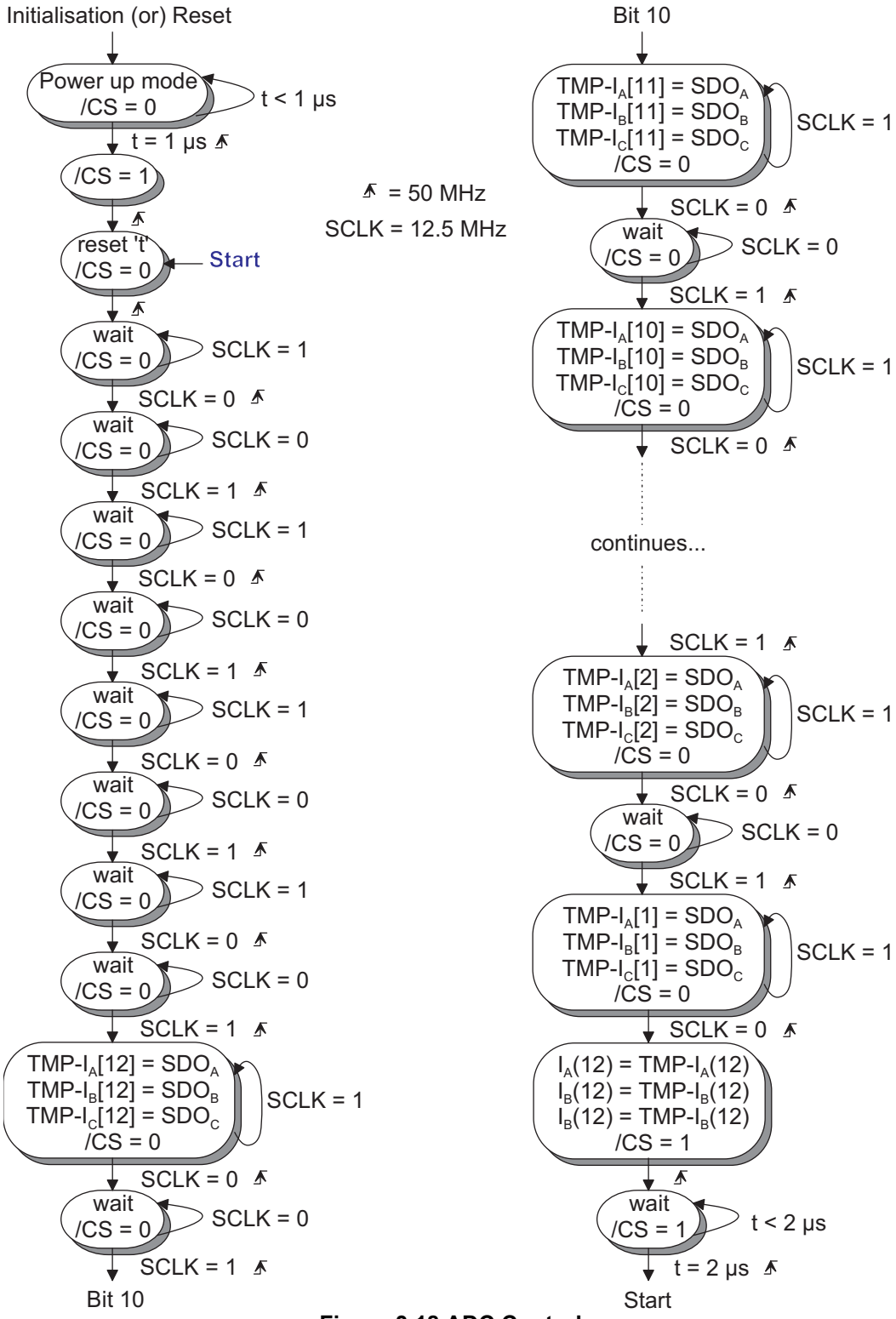


Figure 3.18 ADC Control

3.4.2 Encoder counter control

The signs of the sine and cosine signals are determined using hysteresis comparators. As can be seen in Figure 3.19, four quarter periods (q_0, q_1, q_2 and q_3) can be distinguished within each period using only the signs [59]. The coarse position is calculated by counting the encoder periods. The resolution is the fourfold of the encoder's line count (here, 5000 line counts * 4 = 20000). The coarse position alone is already sufficient to measure the angular position (β) for the speed control.

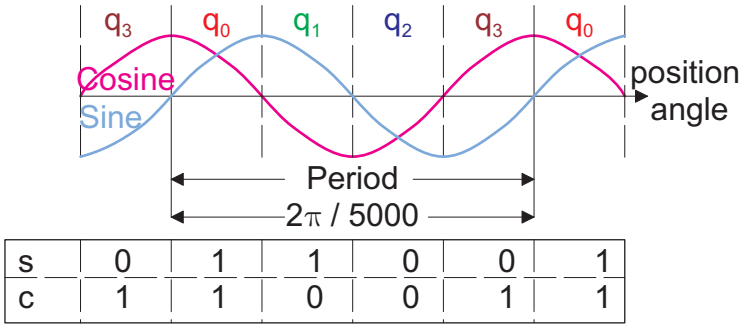


Figure 3.19 Encoder signals

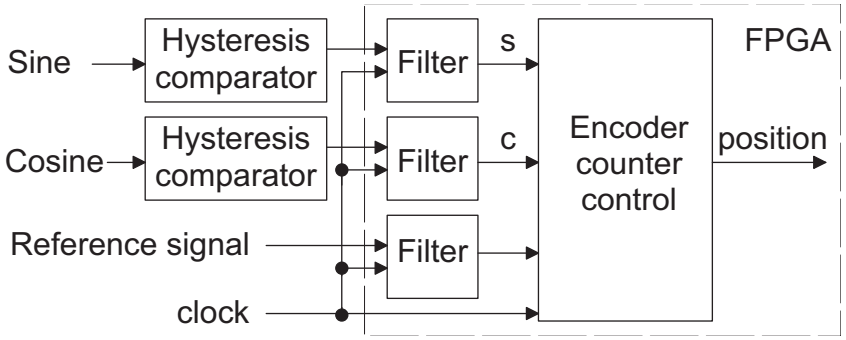


Figure 3.20 Block diagram of a decoder circuit

The periods are counted based on the output of hysteresis comparators. The number of whole encoder periods passed is stored by a counter. The count will be incremented in one direction and decremented in the reverse direction when the shaft is rotating. Filters are used to reject the noise from the multiple inputs. If and only if three consecutive samples have the same value, the output is considered stable and the value is output from the filter [60]. A 50 MHz clock is used. 1500 RPM is the nominal speed of the motor. The reference signal resets the position counter. Figure 3.20 shows the block diagram of a decoder circuit. The implementation of the encoder counter control in FPGA is as shown in Figure 3.21. The counter is incremented/decremented by value 0/1/2 depending upon the filter outputs 's' and 'c'.
The states of the encoder counter control are briefly described below:

- q_0 up – quadrant 'q_0' where signs of the sine and cosine are positive. Here, position counter is counting up.
- q_1 up – quadrant 'q_1' where the sign of a sine is positive and cosine is negative. Here, position counter is counting up.
- q_2 up – quadrant 'q_2' where signs of the sine and cosine are negative. Here, position counter is counting up.
- q_3 up – quadrant 'q_3' where the sign of a sine is negative and cosine is positive. Here, position counter is counting up.
- q_0 dn – quadrant 'q_0' where signs of the sine and cosine are positive. Here, position counter is counting down.
- q_1 dn – quadrant 'q_1' where the sign of a sine is positive and cosine is negative. Here, position counter is counting down.
- q_2 dn – quadrant 'q_2' where signs of the sine and cosine are negative. Here, position counter is counting down.
- q_3 dn – quadrant 'q_3' where the sign of a sine is negative and cosine is positive. Here, position counter is counting down.

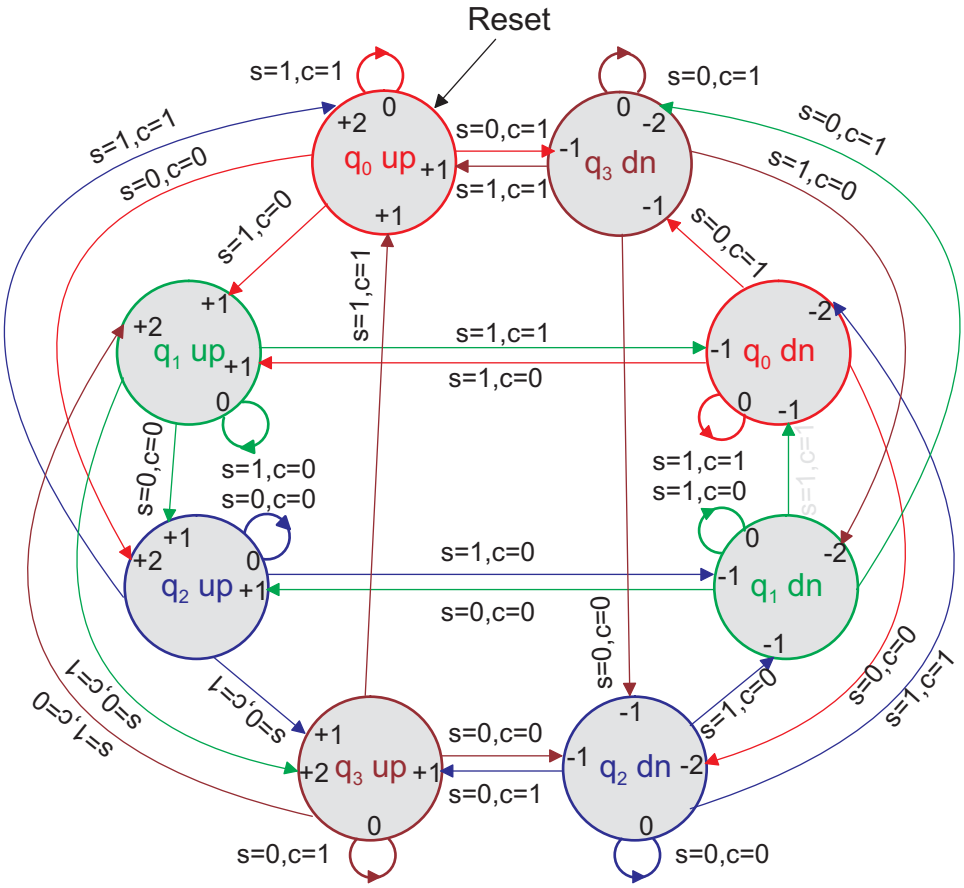


Figure 3.21 Encoder counter control

3.4.3 Speed calculation

The angle measured by the encoder is differentiated with respect to time, so that speed information results. That leads to substantial noise in the high frequency range, which would disturb the control. Therefore, the speed information must be smoothed additionally [59]. A low-pass filter is used for this purpose. The differentiation is implemented together with the low-pass filter of first order, which computes the speed signal from the position.

$$F(s) = \frac{\omega(s)}{\beta(s)} = \frac{s}{1 + sT_f} \tag{3.1}$$

T_f is time constant of a low-pass filter. The bilinear transformation (3.2) is used to transfer the continuous time system to a discrete time system. Here, T is the sampling time.

$$s \rightarrow \frac{2\left(1 - z^{-1}\right)}{T\left(1 + z^{-1}\right)} \tag{3.2}$$

$$\omega[nT] = \frac{2}{T + 2T_f}\left(\beta[nT] - \beta[(n-1)T]\right) - \frac{T - 2T_f}{T + 2T_f}\omega[(n-1)T] \tag{3.3}$$

The discrete time equation (3.3) is used to calculate the speed in FPGA. To implement the multiplication in FPGA, Altera's *lpm_mult* megafunction is used.

3.4.4 Speed reference value filter

With the speed reference value filter (3.4), we eliminate the zero in the transfer function of the speed control loop and get rid of the resonance.

$$F_f(s) = \frac{y(s)}{x(s)} = \frac{\omega^*_{ref}(s)}{\omega_{ref}(s)} = \frac{1}{1 + sT_C} \tag{3.4}$$

T_C is time constant of the speed control. The bilinear transformation (3.2) transfers equation (3.4) to a discrete time system (3.5).

$$y[nT] = \frac{T}{T + 2T_f}\left(x[nT] + x[(n-1)T]\right) - \frac{T - 2T_f}{T + 2T_f}y[(n-1)T] \tag{3.5}$$

3.4.5 The abc to dq transformation & dq to αβ transformation

By using Clarke transformation, the current transformation is given below:

$$i_\alpha = \left(2i_a - i_b - i_c\right)/3 \tag{3.6}$$

$$i_\beta = \left(i_b - i_c\right)/\sqrt{3} \tag{3.7}$$

By using Park transformation,

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta \tag{3.8}$$

$$i_q = -i_\alpha \sin\theta + i_\beta \cos\theta \tag{3.9}$$

The outputs of this block are the flux component current (i_d) and torque component current (i_q). Each of them is controlled by a PI controller.
By using inverse Park transformation, the voltage transformation is given below:

$$V_\alpha = V_d \cos\theta - V_q \sin\theta \tag{3.10}$$

$$V_\beta = V_d \sin\theta + V_q \cos\theta \tag{3.11}$$

The outputs of this block are the components of the reference vector to be applied to the motor.

Cyclone III chip has embedded memory. A sine lookup table with 1024 digital samples (each 16-bit wide) for 360° is created and stored in the memory. The output sin (θ) that corresponds to the input (θ) is generated by using the following equation:

$$\text{lookuptable data} = \left(2^{15} - 1\right)\sin\left(\frac{360°}{1024}n\right),\ n = 0...1023 \tag{3.12}$$

A 0..360° sin lookup table needs more embedded memory but lesser additional math compare to a 0..90° sin lookup table. The Altera's *altsyncram* megafunction is used to read the data from the memory. For multiplication Altera's *lpm_mult* megafunction function is used.

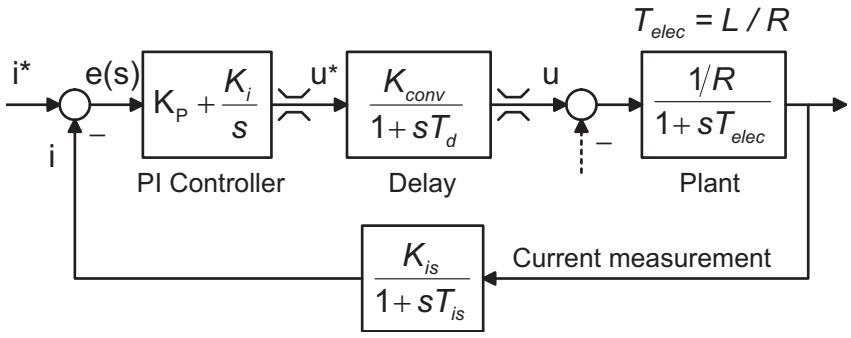


Figure 3.22 Simplified current control loop

3.4.6 PI current control

Figure 3.22 shows the simplified current control loop using a PI controller, where the coupling inductances between the d-q axes were neglected. The control's time delay (included inverter reaction time) is modeled as a first order lag element with a time constant T_d = 1.5T_s where T_s is the sampling time [57]. The converter gain K_{conv} is the relation between the numerical evaluation in FPGA and the real output voltage. In this case, the resolution scale used was 16383 (14 bits) for the complete line to line voltage (2/3 DC-link voltage). Then, K_{conv} is obtained from (3.13). Similarly, K_{is} is the scaling factor of current measurement block and is obtained from (3.14). T_{is} is the current filter time constant, and it is zero in our case. T_{elec} = L/R is the electrical time constant of the motor.

$$K_{conv} = \frac{2/3 V_{dc}}{16383} = 0.0228 \quad \text{for } V_{dc} = 560\,V \tag{3.13}$$

$$K_{is} = \frac{16383}{33.333} = 491.5 \tag{3.14}$$

The defining equations for a PI-controller are as follows:

$$u(t) = K_p e(t) + K_i \int e(t) \tag{3.15}$$

$$x(t) = K_i \int_{t_0}^{t} e(t) + x(t_0) \tag{3.16}$$

The digital realization of the PI-controller using the simple trapezoidal rule for integration is as follows:

$$x[nT_S] = K_i \frac{T_S}{2}\left(e[nT_S] + e[(n-1)T_S]\right) + x[(n-1)T_S] \tag{3.17}$$

$$u[nT_S] = K_P e[nT_S] + x[nT_S] \tag{3.18}$$

This trapezoidal approximation is more accurate than the rectangular approximation. The PI controller is tuned using the criteria of amplitude optimum [58]. Then, the controller coefficients are given by (3.19) and (3.20).

$$K_p = \frac{RT_{elec}}{2T_d K_{is} K_{conv}} \tag{3.19}$$

$$K_i = \frac{R}{2T_d K_{is} K_{conv}} \tag{3.20}$$

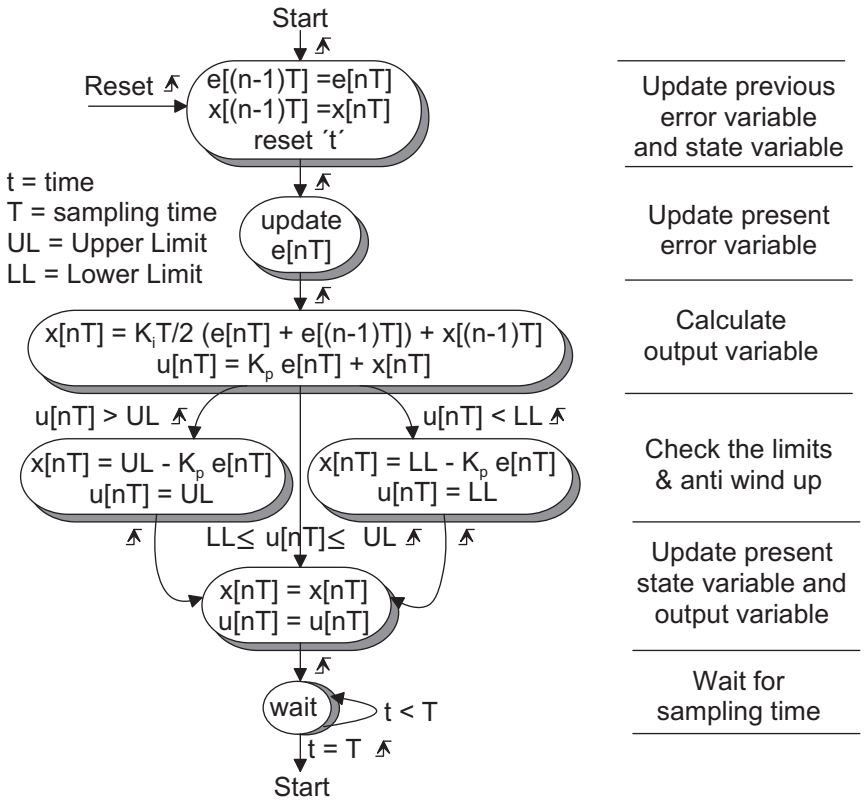


Figure 3.23 State diagram for a PI-controller

Figure 3.23 shows a state diagram for a FPGA PI-controller, including an anti-windup process. The current PI controller samples the data for every 50 µs. The numbers in the FPGA are entered as signed integers. High scaling factor provides high resolution. High resolution consumes more logic cells. A compromise is needed between the resolution and the number of logic cells. The scaling factor 2^{14} provides a good resolution. So the coefficients $K_{p\text{-}FPGA}$ and $K_{i\text{-}FPGA}$ are:

$$K_{p-FPGA}(18\text{ bits}) = K_p * 2^{14} = 73143 \tag{3.21}$$

$$K_{i\_FPGA}(18\text{ bits}) = K_i \frac{T_S}{2} * 2^{14} = 736 \tag{3.22}$$

3.4.7 PI speed control

Figure 3.24 shows the simplified speed control loop using a PI controller. The reference speed is available from the speed reference value filter block and the measured speed is available from the speed calculation block. The speed PI controller samples the data for every 100 µs.

The error vector $e(s)$ is defined as the difference between the reference and the measured values of the controlled speed. The resolution scale used for speed was 16383 (14 bits) for the nominal speed (2.π.1500/60. n_p rad/s).The constant n_p is the number of pole pairs. The output of the PI-controller is the torque component current reference (I_{qref}). So the multiplication factor ($2L_2$ / $I_{dref}.M^2.3n_p$) in (3.23) converts the torque to the corresponding current component. In this case, the flux component current reference (I_{dref}) is constant and is equal to the rated value.

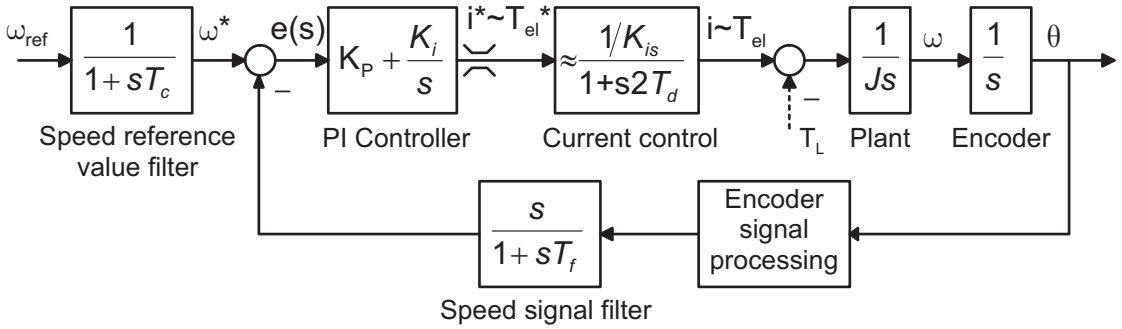


Figure 3.24 Simplified speed control loop

As in the PI current control, the digital realization of the PI-controller is done using the simple trapezoidal rule for integration. The PI controller is tuned using the criteria of symmetrical optimum [57]. Then, the controller coefficients are given by (3.23) and (3.24).

$$K_p = \frac{JK_{is}}{2T_d + T_f} \cdot \frac{2\pi \frac{1500}{60} n_p}{16383} \cdot \frac{2L_2}{I_{dref} M^2 3 n_P} \tag{3.23}$$

$$K_i = \frac{K_P}{4\left(2T_d + T_f\right)} \tag{3.24}$$

The implementation of a PI speed controller in FPGA is similar to the implementation PI current control and is shown in Figure 3.23.

3.4.8 Calculation of the switching times T_0, T_1 and T_2

In a switching cycle T_s,

$$\left|V_{ref}\right| e^{j\varepsilon_{ref}} T_s = \vec{V}_0 T_0 + \vec{V}_1 T_1 + \vec{V}_2 T_2 \tag{3.25}$$

The time T_0 is the on-time of a zero voltage vector ($\vec{V}_0$ or $\vec{V}_7$). The active vectors $\vec{V}_1$ and $\vec{V}_2$ on time durations are T_1 and T_2.

From the voltages (V_α and V_β), using conventional SVPWM, switching times T_0, T_1 and T_2 are calculated within a switching period T_S [61]. For a sector (s) = 1,

$$\frac{T_1}{T_S} = V_\alpha - \frac{1}{\sqrt{3}} V_\beta; \quad \frac{T_2}{T_S} = \frac{2}{\sqrt{3}} V_\beta; \quad \frac{T_0}{T_S} = 1 - \frac{T_1}{T_S} - \frac{T_2}{T_S} \tag{3.26}$$

Where $V_\alpha = \left|V^*_{ref}\right| \cos \varepsilon_{ref}$, $V_\beta = \left|V^*_{ref}\right| \sin \varepsilon_{ref}$

The coefficients of V_α and V_β vary with respect to the sector. Then the switching times can be expressed as:

$$\frac{T_1}{T_S} = C_{11} V_\alpha - C_{12} V_\beta; \frac{T_2}{T_S} = C_{21} V_\alpha - C_{22} V_\beta; \frac{T_0}{T_S} = 1 - \frac{T_1}{T_S} - \frac{T_2}{T_S} \tag{3.27}$$

Depending upon V_α and V_β, the sector number (s) and coefficients C_{11}, C_{12}, C_{21} and C_{22} are calculated as in [61]. Integer coefficients for different sectors are given in Table 3.2. Here the digital equivalent for 1 per unit is 16383 (14 bits).

Table 3.2: Coefficients of V_α and V_β

Condition	Sector	C_{11}	C_{12}	C_{21}	C_{22}
$V_\alpha\,[MSB] = 0,\ V_\beta\,[MSB] = 0,\ V_\beta < \sqrt{3}\,V_\alpha$	1	*16383*	*−9459*	0	*18918*
$V_\alpha\,[MSB] = 0,\ V_\beta\,[MSB] = 0,\ V_\beta \geq \sqrt{3}\,V_\alpha$	2	-16383	9459	16383	9459
$V_\alpha\,[MSB] = 1,\ V_\beta\,[MSB] = 0,\ V_\beta \geq -\sqrt{3}\,V_\alpha$	2	-16383	9459	16383	9459
$V_\alpha\,[MSB] = 1,\ V_\beta\,[MSB] = 0,\ V_\beta < -\sqrt{3}\,V_\alpha$	3	0	18918	-16383	-9459
$V_\alpha\,[MSB] = 1,\ V_\beta\,[MSB] = 1,\ V_\beta > \sqrt{3}\,V_\alpha$	4	0	-18918	-16383	9459
$V_\alpha\,[MSB] = 1,\ V_\beta\,[MSB] = 1,\ V_\beta \leq \sqrt{3}\,V_\alpha$	5	-16383	-9459	16383	-9459
$V_\alpha\,[MSB] = 0,\ V_\beta\,[MSB] = 1,\ V_\beta \leq -\sqrt{3}\,V_\alpha$	5	-16383	-9459	16383	-9459
$V_\alpha\,[MSB] = 0,\ V_\beta\,[MSB] = 1,\ V_\beta > -\sqrt{3}\,V_\alpha$	6	16383	-9459	0	-18918

*MSB = Most Significant Bit.

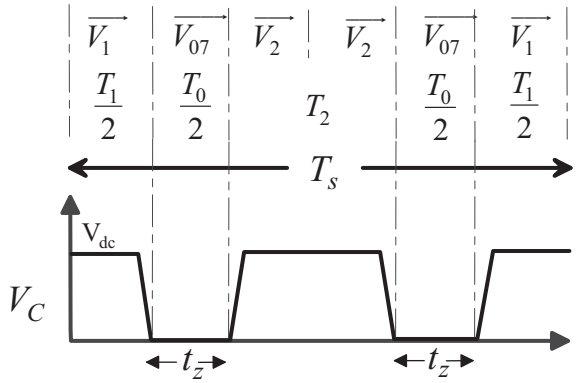


Figure 3.25 Modified Space Vector Modulation

3.4.9 Calculation of modified switching times

The quasi-resonant dc-link inverter changes the switching pattern under zero voltage condition. It is explicit that the resonant operation requires minimum time for current built-up, the resonant oscillation, zero voltage interval and the restoring to V_{dc}. It imposes a condition that the PWM pulse widths should be longer than the required minimum pulse duration. In the conventional space vector modulation, it requires 6 resonant cycles per switching period T_S, resulting in poor DC-link voltage utilization. A different modulation technique is adopted for better utilization of DC-link voltage and common mode voltage reduction (section 2.4.1).

Figure 3.25 shows a modified modulation where each active vector is followed by a zero vector. A zero vector is effectively equivalent to the zero voltage period (t_z) generated by the resonant cycle. In order to accommodate the zero vector, the zero voltage period (t_z) can be extended (Figure 3.25). So the modified space vector modulation requires only 2 resonant cycles per switching period T_S.

The implementation of this modulator in a FPGA seems, at a first glance, to be rather simple. However, several important issues have to be taken care. In order to implement the resonant cycle between the two active vectors, the following facts have to be considered:

1. One resonant cycle should be finished before the next one starts.

2. Short active vector on-times have to be eliminated.

The width of the resonant cycle is dependent on the load current and the resonant elements. For the given resonant elements and the maximum load current, the maximum time to complete one resonant operation does not exceed T_{res} (without extending the zero voltage period t_z). So T_{res} is the time to complete one resonant cycle, without extending the zero voltage period t_z.

Case 1: From Figure 3.25, we can derive the following constraints:

$$T_0/2 + T_1 \geq T_{res} \tag{3.28}$$

$$T_0/2 + T_2 \geq T_{res} \tag{3.29}$$

- If (3.28) is not fulfilled, i.e. if $T_0/2 + T_1 \leq T_{res}$, then the active vector T_1 is dropped to zero and this time is added to T_0. The equation (3.25) is modified as $|V_{ref}|e^{j\varepsilon_{ref}}T_s = \vec{V}_0(T_0 + T_1) + \vec{V}_2T_2$. The zero voltage period (t_z) is extended to $T_0 + T_1$.
- If (3.29) is not fulfilled, i.e. if $T_0/2 + T_2 \leq T_{res}$, then the active vector T_2 is dropped to zero and this time is added to T_0. The equation (3.25) is modified as $|V_{ref}|e^{j\varepsilon_{ref}}T_s = \vec{V}_0(T_0 + T_2) + \vec{V}_1T_1$. The zero voltage period (t_z) is extended to $T_0 + T_2$.

For the above mentioned cases, the resonant operation started will not be completed before the next one starts. So the short vectors are dropped and added to zero voltage period. It results in one resonant cycle instead of two cycles in a switching period T_s. The following algorithm is implemented in FPGA:

If $T_0/2 + T_1 \leq T_{res}$ *and* $T_0/2 + T_2 \leq T_{res}$,
Then $T_1^M = 0_1, T_2^M = 0, T_0^M = T_0 + T_1 + T_2$
Else if $T_0/2 + T_1 \leq T_{res}$,
Then $T_1^M = 0, T_2^M = T_2, T_0^M = T_0 + T_1$
Else if $T_0/2 + T_2 \leq T_{res}$,
Then $T_1^M = T_1, T_2^M = 0, T_0^M = T_0 + T_2$

Case 2: When the reference vector lies near to the boundaries of the sector, T_1 and T_2 are too short. For this case, the vector dropping algorithm described in [63] is used. T_{min} is the required minimum on-time of a voltage vector.

- If $0 < T_1 \leq T_{min}/2$, then the active vector T_1 is dropped to zero and this time is added to T_0. The new zero voltage period (t_z) is $T_0 + T_1$.
- If $T_{min}/2 < T_1 \leq T_{min}$, then the active vector T_1 is prolonged to T_{min} and the added time is subtracted from T_0. The new zero voltage period (t_z) is $T_0 - (T_{min} - T_1)$.
- If $0 < T_2 \leq T_{min}/2$, then the active vector T_2 is dropped to zero and this time is added to T_0. The new zero voltage period (t_z) is $T_0 + T_2$.
- If $T_{min}/2 < T_1 \leq T_{min}$, then the active vector T_2 is prolonged to T_{min} and the added time is subtracted from T_0. The new zero voltage period (t_z) is $T_0 - (T_{min} - T_2)$.

The following algorithm is implemented in FPGA:

If $0 < T_1 \leq T_{min}/2$ *and* $0 < T_2 \leq T_{min}/2$,
Then $T_1^M = 0_1, T_2^M = 0, T_0^M = T_0 + T_1 + T_2$
Else if $0 < T_1 \leq T_{min}/2$,

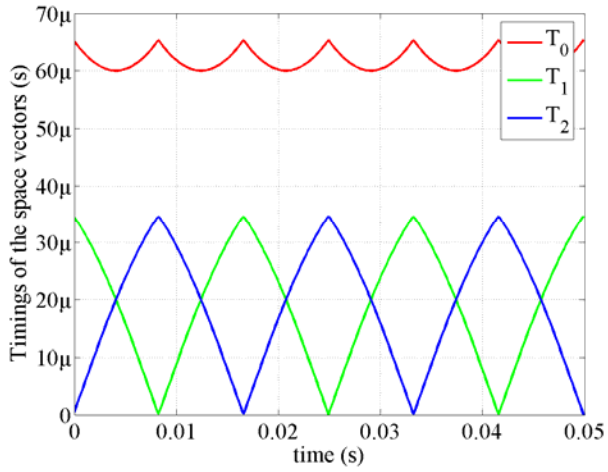


Figure 3.26 Switching times of space vectors for constant frequency 20 Hz

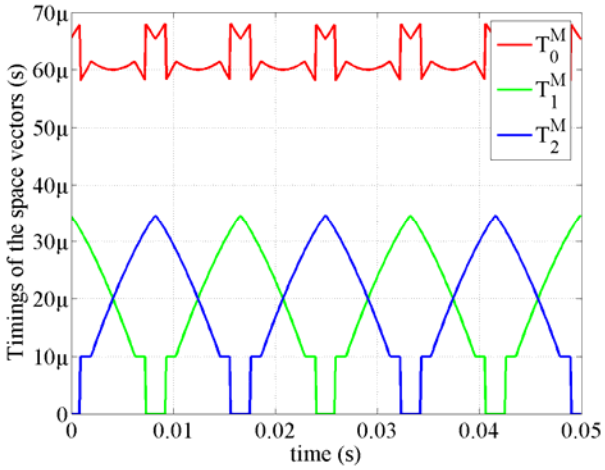


Figure 3.27 Modified switching times for constant frequency 20 Hz

Then $T_1^M = 0, T_2^M = T_2, T_0^M = T_0 + T_1$

Else if $0 < T_2 \le T_{min}/2$,

Then $T_1^M = T_1, T_2^M = 0, T_0^M = T_0 + T_2$

Else if $0 < T_1 \le T_{min}/2$ *and* $T_{min}/2 < T_2 \le T_{min}$,

Then $T_1^M = 0, T_2^M = T_{\min}, T_0^M = T_0 + T_1 + T_2 - T_{\min}$

Else if $0 < T_2 \le T_{min}/2$ *and* $T_{min}/2 < T_1 \le T_{min}$,

Then $T_1^M = T_{\min}, T_2^M = 0, T_0^M = T_0 + T_1 + T_2 - T_{\min}$

Else if $T_{min}/2 < T_1 \le T_{min}$,

Then $T_1^M = T_{\min}, T_2^M = T_2, T_0^M = T_0 + T_1 - T_{\min}$

Else if $T_{min}/2 < T_2 \le T_{min}$,

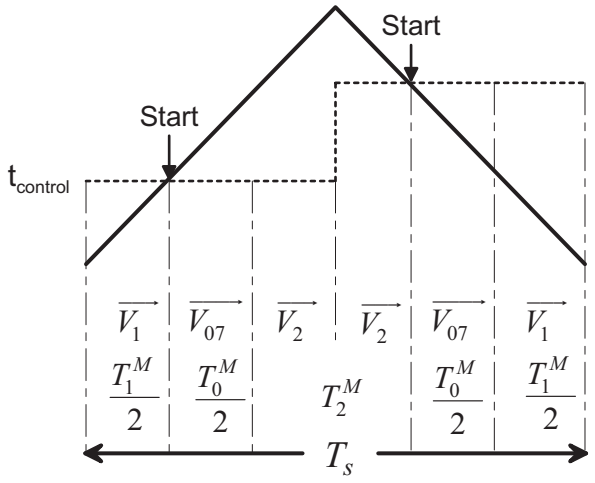
Then $T_1^M = T_1, T_2^M = T_{\min}, T_0^M = T_0 + T_2 - T_{\min}$

If the active vector is too short ($\le T_{min}/2$), it is dropped to zero, and this time is added to T_0. If the active vector is short ($> T_{min}/2$ & $\le T_{min}$), it is prolonged to T_{min}, and the added time is subtracted from T_0.

The switching frequency (f_s) is 10 kHz, leading to a switching period (T_s) of 100µs. The maximum time (T_{res}) to complete one resonant cycle is 16µs. The required minimum on-time of a voltage vector (T_{min}) is 10 µs. Figure 3.26 is the graphical representation of the timings T_0, T_1 and T_2 for one cycle of constant frequency 20 Hz. The modified switching times T_0^M, T_1^M and T_2^M are shown in Figure 3.27.

3.4.10 Control of a resonant circuit and inverter bridge

Whenever a change in the switching status is needed, a 'Start' signal is generated. It initiates a resonant cycle. For sector 1, the 'Start' signal generation is shown in Figure 3.28. When the signal $t_{control}$ is equal to the triangle carrier, a resonant cycle will be initiated. The end of a resonant cycle is determined by resonant circuit parameters, load current, trip currents and modified zero vector time T_0^M. The triangle carrier has a frequency (f_s) of 10 kHz and amplitude of T_s / 2. The state diagram for resonant link control is shown in Figure 3.29. The zero voltage period (t_z) is calculated in section 3.4.9.



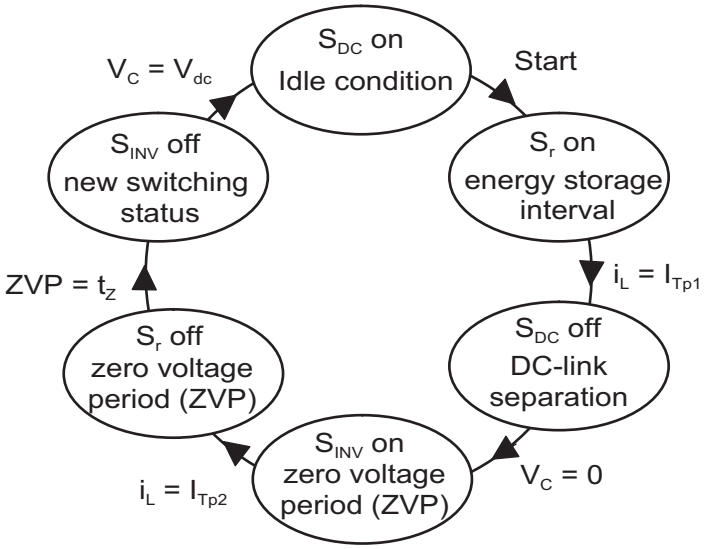
Traingular carrier rise time:

$$t_{control} = \frac{T_1^M}{2}$$

Traingular carrier fall time:

$$t_{control} = \frac{T_0^M}{2} + \frac{T_1^M}{2}$$

Figure 3.28 PWM (Sector 1 : Start signal generation)



S_{DC} on = S_{DC1} on, S_{DC2} on

S_{DC} off = S_{DC1} off, S_{DC2} off

Start = Starting of a resonant cycle

t_Z = zero voltage period

Figure 3.29 State diagram for Quasi Resonant DC-link inverter Control

If $T_1^M > 0$ and $T_2^M > 0$, then $t_Z = T_0^M/2$. If $T_1^M = 0$ or $T_2^M = 0$, then $t_Z = T_0^M$. It results in one resonant cycle instead of two cycles in a switching period T_s.

3.4.11 Trip currents look up table

The trip currents are a function of inverter input currents (I_O and I_{OX}) and other circuit parameters (section 2.3.1). The resonant cycle is heavily influenced by the initial load current I_O and the next load current I_{OX}. These inverter input currents are predicted in the FPGA from the following equations [40]:

$$I_O = S_1 i_a + S_3 i_b + S_5 i_c \tag{3.30}$$

$$I_{OX} = S_{1X} i_a + S_{3X} i_b + S_{5X} i_c \tag{3.31}$$

Where S_1, S_3, S_5 are the Boolean variables of switches, which correspond to '0' or '1' depending upon the state of the inverter switches. A conducting switch corresponds to '1', and an off-state switch corresponds to '0'. S_{1X}, S_{3X}, S_{5X} are the next switching states after completion of resonant operation. The largest possible value for the inverter input currents (I_O and I_{OX}) is the peak value of a phase current (without noise).

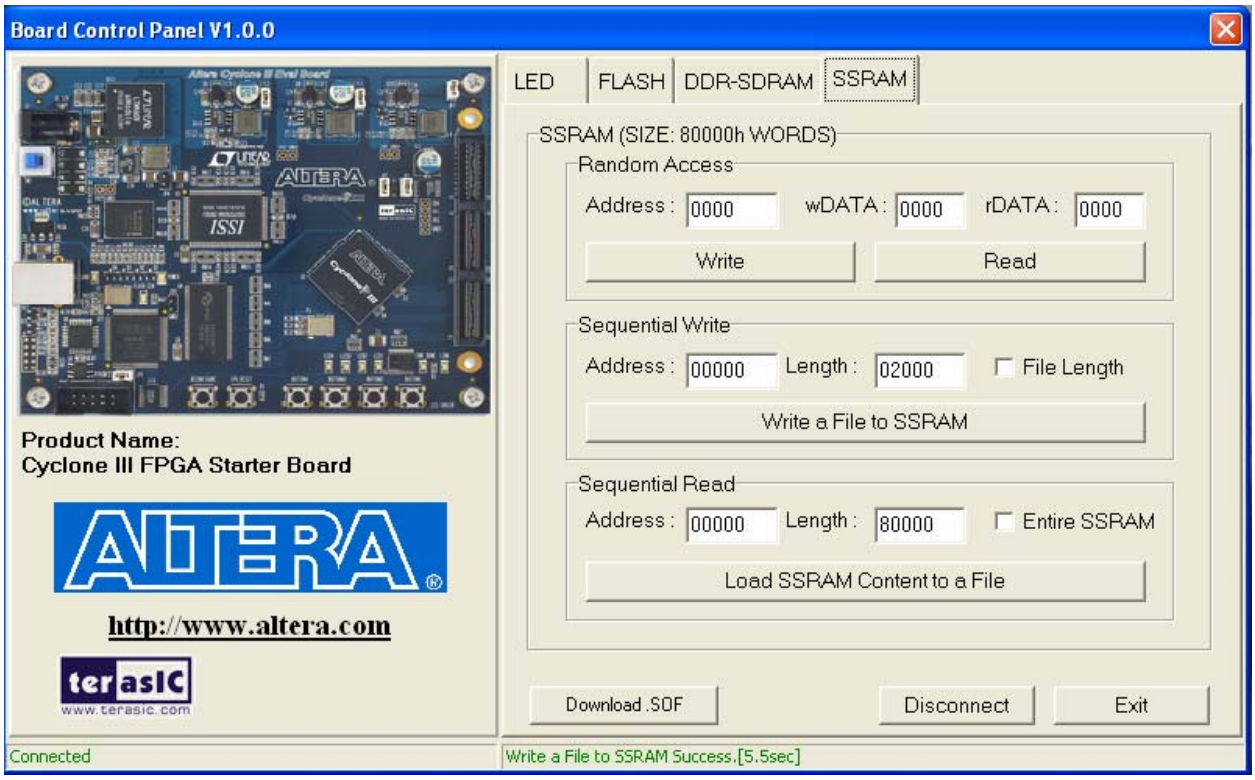


Figure 3.30 Control panel

Table 3.3: SSRAM I/O in continuous read mode

SSRAM (IS64LPS25636A)	
Synchronous clock (clock)	50 MHz
Output enable (/OE)	GND
Synchronous chip enable (/CE)	GND
Synchronous byte write enable (/BWE)	GND
Synchronous byte write enable (/BWa - /BWd)	GND
Synchronous control address status (/ADSC)	GND
Address input [6..1] (6 bit)	I_O [12..7] (upper 6 bit ≈ steps of 1.042 A)
Address input [12..7] (6 bit)	I_{OX} [12..7] (upper 6 bit ≈ steps of 1.042 A)
Address input [21..13] (9 bit)	0
Data output [16..1] (16 bit)	I_{Tp1}
Data output [32..17] (16 bit)	I_{Tp2}

The maximum value that can be stored in the inverter input current registers (12 bit) is 33.33 A, which comes from the current measurement block. Trip currents are calculated in MATLAB for different inverter input currents (in steps of 1.042 A from - 33.33 A to 33.33 A). With step size less than 1.042 A, change in the trip current's value is negligible. Lesser the step size, higher memory space is needed to store the trip currents. The cyclone III

FPGA starter board has a 256K*32 synchronous SRAM [71]. The off-line calculated trip currents (I_{Tp1} and I_{Tp2}) are stored in this memory with the help of the control panel provided by Altera (Figure 3.30) [72]. Memory used to store both the trip currents is 16384 bytes.

Before every switching, the load currents I_O and I_{OX} are calculated in the FPGA. Depending upon the load currents, the trip currents I_{Tp1} and I_{Tp2} are recalled from the memory. A two dimensional (2D) lookup table is needed to read the data from the memory. A SSRAM driver program is written in the FPGA with an address input (21 bit) and data output (32 bit). Instead of using multiplexers for 2D lookup table, the memory address is divided into two parts. The two parts represent the currents I_O and I_{OX} respectively (Table 3.3). It is less complicated and requires fewer number of logic cells. In a continuous read mode, the input and outputs to and from the SSRAM memory are given in Table 3.3. The trip current is recalled beforehand and given to the digital to analog control (DAC).

3.4.12 Monitoring

Figure 3.31 shows the monitoring state machine implemented in the FPGA. This state machine is updated with 50 MHz clock. As the name indicated, this block monitors the signals and in case of fault it disconnects the DC link capacitor from the inverter bridge. Initially, the reset is active and all the blocks are inactivated. Pressing the 'Button 1' makes the reset zero and all the blocks active. Then the control signals are generated by the FPGA.

The MOSFET switches S_{DC1} and S_{DC2} connect the inverter bridge to the DC link voltage. From the time, the program is loaded into the FPGA the turn-on command is given to the switches S_{DC1} and S_{DC2}. These switches are turned-off either during resonant operation or in case of any faults (DC link = OFF in Figure 3.31). The faults are indicated by the different status of the LEDs on the FPGA starter kit. The LED blink time is set to 5s by using a counter.

Desaturation detection is done on the inverter board. The fault signal ($f1$) is reported to the FPGA through the interface board. Filter is used to reject the noise. If and only if eight consecutive samples have the same value, the output is considered stable and the value is output from the filter, i.e. $F1$.

The measured speed is compared against the nominal speed in FPGA. Similarly, over current protection is done on the board. The measured currents are compared against the nominal currents and if the fault persists for more than 6 µs, an error is reported. In this case, inverter bridge switches are also opened.

The resonant circuit is protected by measuring the inductor current and comparing against a reference value. It was done on the interface board and error $f4$ is reported to the FPGA. The signal is filtered against the noise as in the case of desaturation detection fault signal.

The resonant cycle is completed based on the feed backs of the variables resonant inductor current (i_L) and inverter bridge input voltage (V_c). If the resonant cycle is taking much longer time than it should be, the modulator block sends a fault signal to the monitor block. The maximum time to complete a resonant cycle is set to 110 µs.

3.5 Conclusions

The semiconductor devices CoolMOS, ESBT and IGBT4 have been investigated regarding their suitability for resonant circuit. Due to short switching times, the CoolMOS are optimal to be used as S_{DC1} and S_{DC2}. IGBT4 power semiconductor is suited for S_r due to low conduction losses, high breaking voltage and small stray collector-emitter capacitance. In this chapter, the control of a resonant circuit based on the acquisition of

voltage and current signals is discussed. The total control of a soft switching inverter together with the motor has been realized in a single chip FPGA (Field Programmable Gate Array). The resources utilized are listed in Table 3.4.

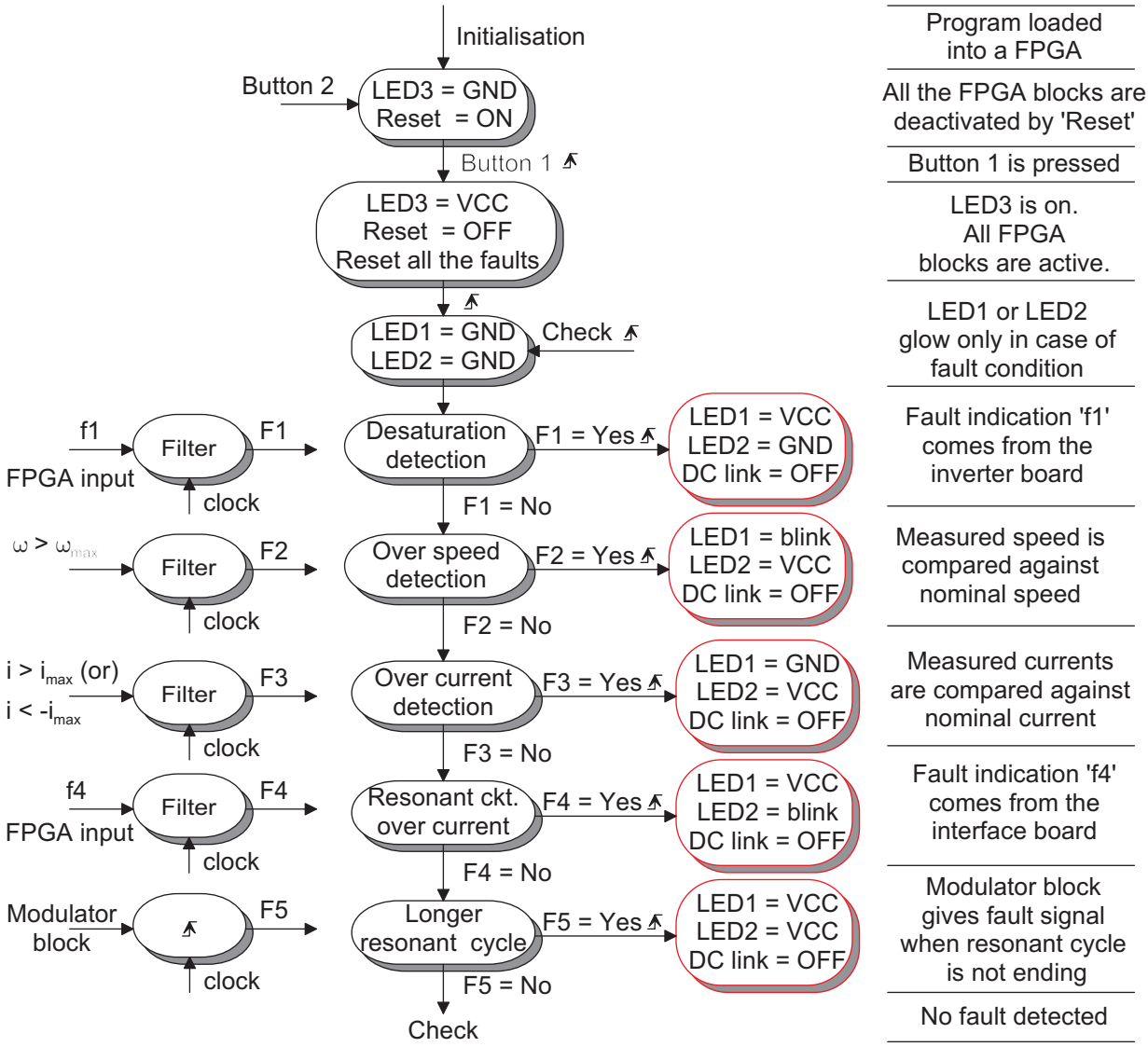


Figure 3.31 Monitoring state machine

Table 3.4: Cyclone III FPGA

Cyclone III (EP3C25F324C8) FPGA starter kit	
Total logical elements	8588 / 24624 (35 %)
Embedded 9-bit multiplier	76 / 132 (58 %)
Total PLLs	1 / 4 (25 %)
Embedded Memory (bits)	163840 / 608256 (27 %)
On Board SSRAM Memory (bytes)	16384 / 1048576 (1.56%)

4 Experimental Results

4.1 Introduction

In this chapter, the performance of a motor friendly QRDCL inverter is verified through an experimental setup and the measurements are presented. Waveforms of the motor friendly characteristics are shown and discussed. The inverter efficiency is measured for the quasi resonant inverter and the hard switching inverter with and without filters. The laboratory setup consists of a 4 kW squirrel cage induction machine with its stator connected to the QRDCL inverter. In order to load the induction motor, a dc generator is coupled to the shaft of the induction motor. The electrical power is fed back to the DC-link capacitor via a 4-quadrant chopper.

4.2 Experimental set-up

Figure 4.1 shows the hardware schematic. The diode bridge is connected to the 415 V, 50 Hz, 3-phase power grid. The inverter is fed from a diode bridge rectifier and 4-Quadrant chopper. The inverter is controlled by using a FPGA. The inverter can operate as both hard switching (HS) and soft switching (SS) inverter. A 34m long LAPP shielded cable is connected between inverter and induction machine.

During the HS inverter mode, DC-link switches S_{DC1} and S_{DC2} are closed and resonant switch S_r is opened perpetually. In order to reduce the parasitic effects for HS inverter, the output filters are connected to the inverter. The efficiency measurements are done with two different filters. In one case, the Schaffner FN510-24-33 output filter is connected in order to reduce the *dv/dt* gradients. In the other case, the EPCOS Sine wave EMC output filter (B84143V0011R127) is connected to reduce the EMC effects.

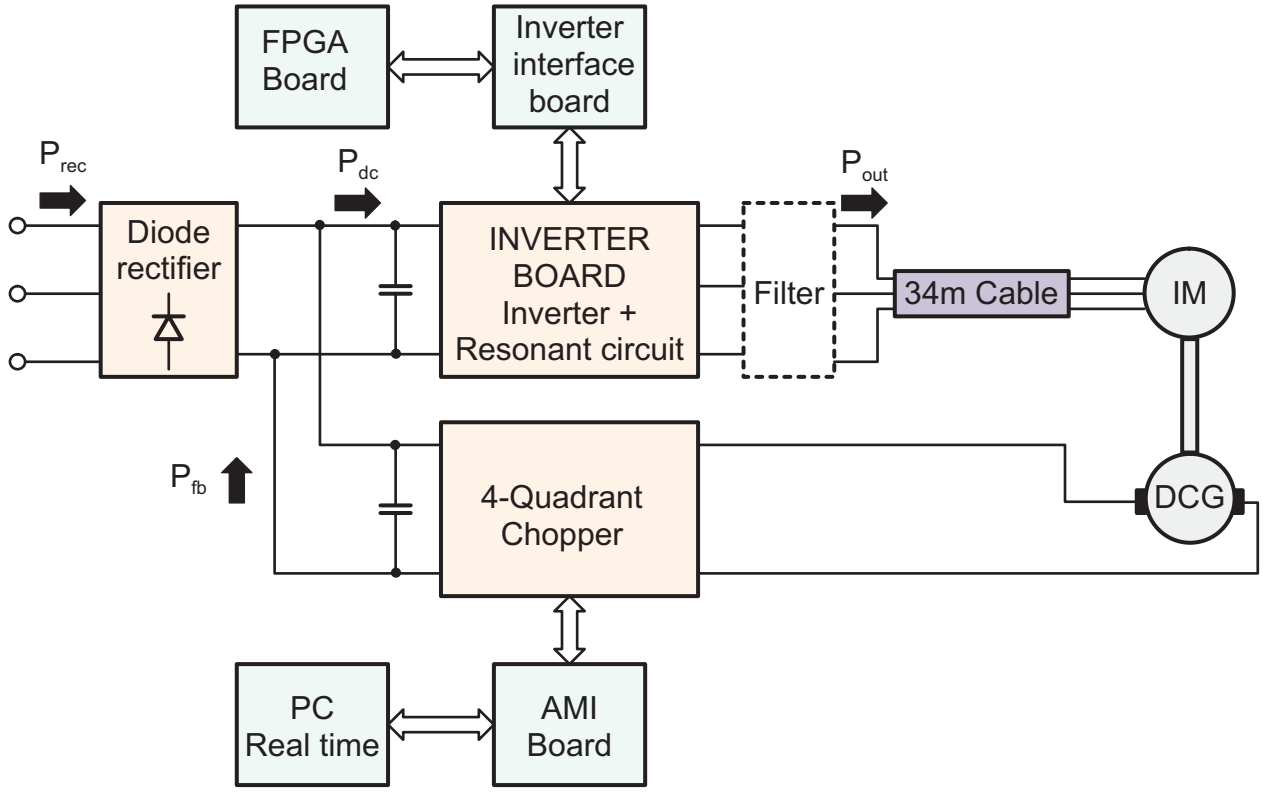


Figure 4.1 Hardware schematic

During the SS inverter mode, the DC-link switches S_{DC1} and S_{DC2} and resonant switch S_r are controlled in such a way to have zero voltage switching. The resonant elements are designed for the maximum inverter output voltage gradient of 600V/μs. With the help of an additional switch and extended resonant cycle, common mode voltage level is also reduced. So the output filters are not needed when the inverter is operating in SS mode. The efficiency is measured for inverter together with resonant circuit, i.e. QRDCL inverter. The hardware setup of the inverter together with the FPGA board and interface board is shown in Figure 4.2.

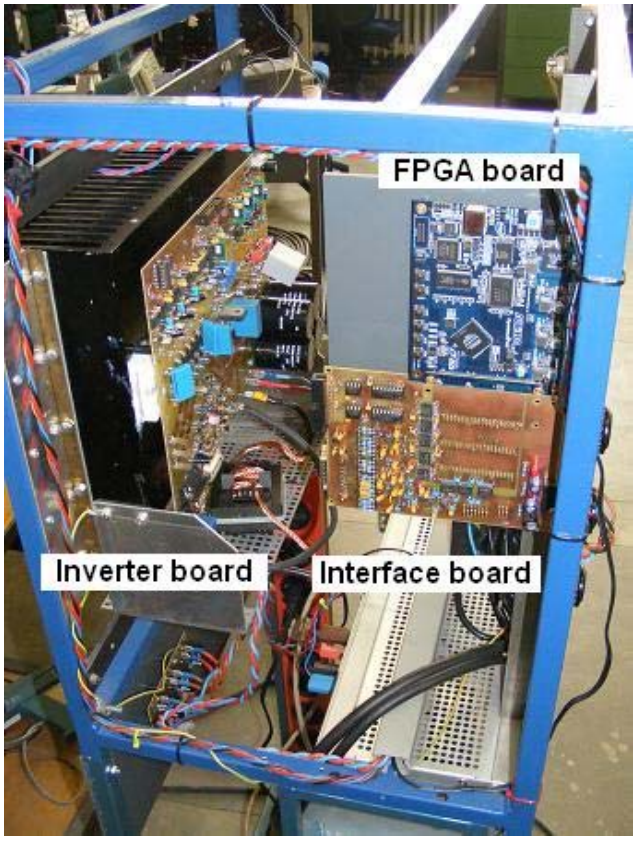


Figure 4.2 Laboratory setup : Inverter board with control unit

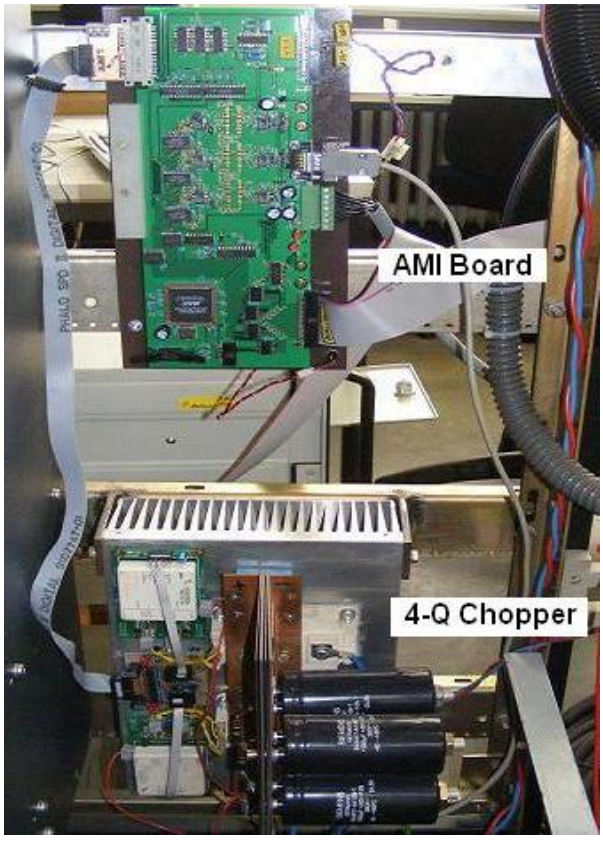


Figure 4.3 Laboratory setup : 4-Q chopper for DC machine braking

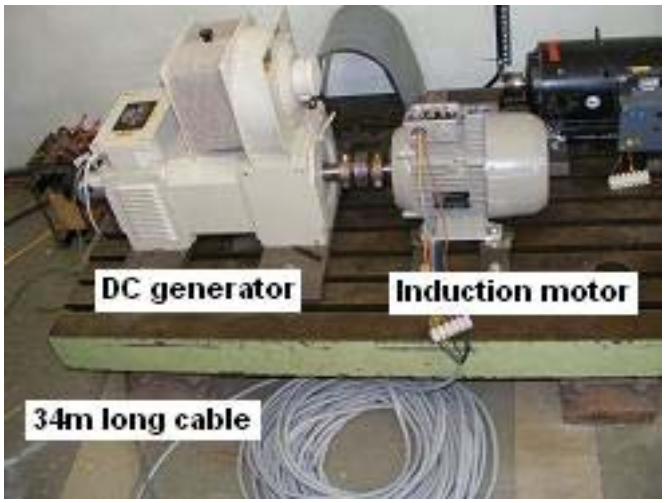


Figure 4.4 Induction motor coupled to DC generator

Figure 4.5 Output filters along with a resonant inductor (in oval)

Table 4.1: Parameters

Siemens 4kW IM parameters (1LE1002-1BB22-2AA0)			Piller 15kW DC motor parameters (GML 112.17V)	
Rated power [kW]	4		Rated power [kW]	15
Rated voltage [V]	400 (Y)		Rated voltage [V] (armature)	400
Rated current [A]	8.2		Rated current [A] (armature)	43
Magnetizing current [A]	4.3		Rated / Maximum voltage [V] (excitation)	70 / 220
Rated torque [Nm]	27			
Rated speed [1/min]	1435		Rated / Maximum current [A] (excitation)	0.85 / 2.5
Power factor	0.84			
Number of poles	4		Rated / Maximum speed [1/min]	3250 / 8000
Cable (LAPP Classic 115CY)				
Number of conductors	5		Conductor's cross section [mm^2]	2.5
Shielded	Yes		Length [m]	34

The induction machine is coupled to a DC generator and loaded electrically (Figure 4.4). The motor parameters are summarized in Table 4.1. The 4 kW induction machine is supplied by an inverter. The DC generator is fed with constant field current, and the armature current is controlled using a 4-Quadrant chopper. The DC-links of QRDCL inverter and of the H-bridge converter (4-Quadrant chopper) are connected together. So the output electrical power is recovered and is used for driving the Induction machine. The chopper is controlled using a real time PC and an AMI (Antrieb Module Interface) board. The AMI board is developed at Technical University Darmstadt [74]. The chopper control program runs under a real time operation system on control PC. The real time core control, communication to the AMI board and AHDL program for SVPWM in CPLD are implemented by [74], [75]. In Figure 4.3, the 4-Q chopper together with AMI board is shown. Figure 4.5 shows the output filters along with the resonant inductor.

4.3 Resonant cycle

In Figure 4.6, the inverter bridge input voltage (V_C), resonant capacitor voltage (V_{Cr}) and resonant inductor current (i_L) are shown. The inverter bridge input voltage (V_C) is made to become zero by resonant operation. The inverter switches change their status within this zero voltage period. For the selected design parameters, the peak voltage (V_{Cr}) on the resonant capacitor will be always less than the DC-link voltage. Even though the peak currents in the resonant inductor are higher, the average value of the resonant inductor current is low.

As discussed in the section 2.4.1 and section 3.4.9, the resonant zero voltage period is used for implementing zero vector intervals of PWM. As the duration of zero vector changes with the modulation index of PWM, the length of a resonant period also changes. At low modulation index, the duration of a zero vector is high and resonant cycles are longer as shown in Figure 4.6 (b). The zero voltage period can be prolonged by keeping shoot-through switching state of the inverter bridge longer.

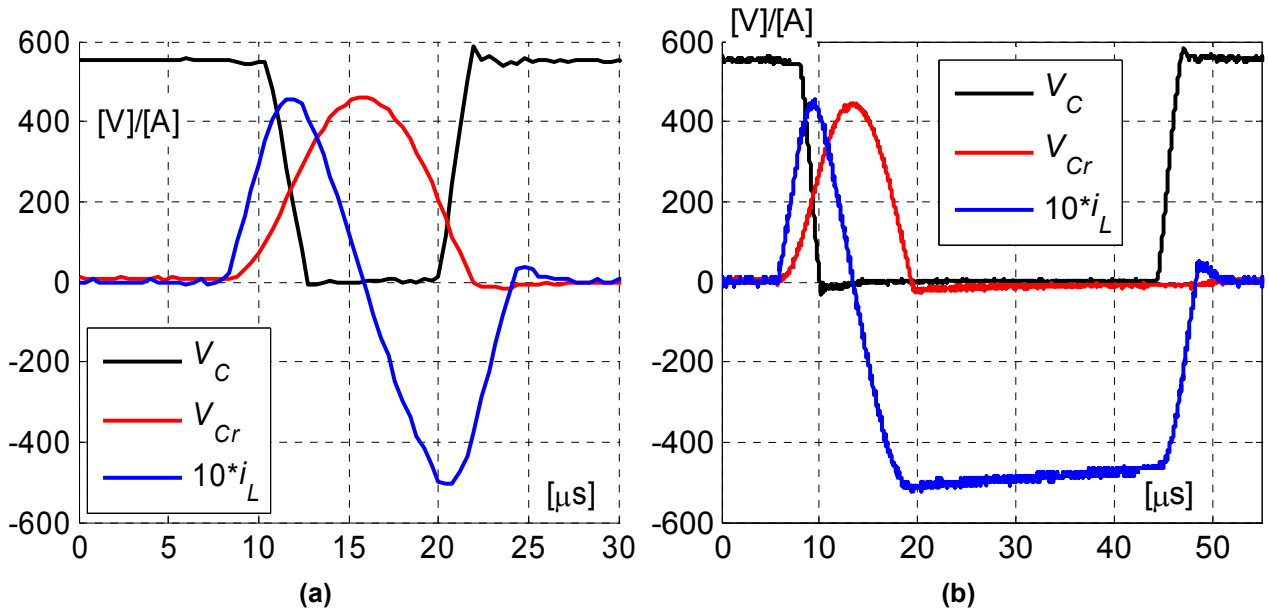


Figure 4.6 Resonant circuit waveforms (a) short resonant cycle (b) long resonant cycle

If we keep all the inverter switches closed further the capacitor voltage V_{Cr} discharges to zero and the total energy is stored in the resonant inductor only. Until we apply the next switching state to the inverter bridge, the inductor current i_L freewheels through the diode D_{r1} and the inverter switches. In ideal case, this current i_L will be constant. But under real conditions, the resonant inductor current (i_L) is slowly decreasing. It is due to the losses in the freewheeling path, i.e. resonant inductor losses, diode (D_{r1}) conduction losses and losses in the inverter bridge. If this decrease in the current is higher, at the end of a resonant cycle, the inverter bridge voltage will not be able to reach the DC-link source voltage again. So the energy stored in the inductor, i.e. the trip current level I_{Tp1} should be increased to compensate these losses. The short and long resonant cycles are shown in Figure 4.6 (a) and (b) respectively. The zero voltage period with different lengths is observed when inverter bridge input voltage (V_C) falls to zero.

4.4 Voltage reflections

After connecting a 34m long LAPP cable between QRDCL inverter and motor, the line to line voltage at the inverter terminals and motor terminals is measured. Because of reduced voltage gradients impressed to the cable, the voltage reflections at load terminals are minimized. The difference of the observed voltage slopes in Figure 4.7 is due to the effect of load currents on the resonant cycle.

The rate of change of a line to line voltage is same as the inverter bridge input voltage. The rate of falling and rising of the inverter bridge input voltage depends not only on resonant elements but also on load currents I_O and I_{OX} respectively. With an increase in the inverter input current I_O, snubber capacitor C is discharged quickly and the voltage V_C decays fast. With the maximum negative inverter input current (I_{OX}), the capacitor C is charged quickly and voltage V_C rises fast. The resonant inverter elements are designed for the worst case, i.e. maximum voltage slope approximately 600 V/µs and the overvoltage at motor terminals below 20% for 34m long LAPP shielded cable.

Figure 4.7 shows the falling edge of a line to line voltage for different load conditions. With load, the motor current is high and the snubber capacitor C will be discharged quickly. With no load, the motor current is small, which is equivalent to the induction machine magnetizing current. So the snubber capacitor C will be no longer

discharged quickly. Voltage peak at motor terminal increases with the slope (Figure 4.7). The DC-link voltage under no load is 600 V and with load is 500 V.

Figure 4.8 shows the rising edge of a line to line voltage for different load conditions. As in the previous case, the voltage rise also depends upon load currents. The ringing in the voltage rise at the inverter terminals is caused by resonance between DC-link stray inductance and snubber capacitor. During the falling edge, this voltage is clamped to zero by the inverter bridge diodes. So no ringing is observed.

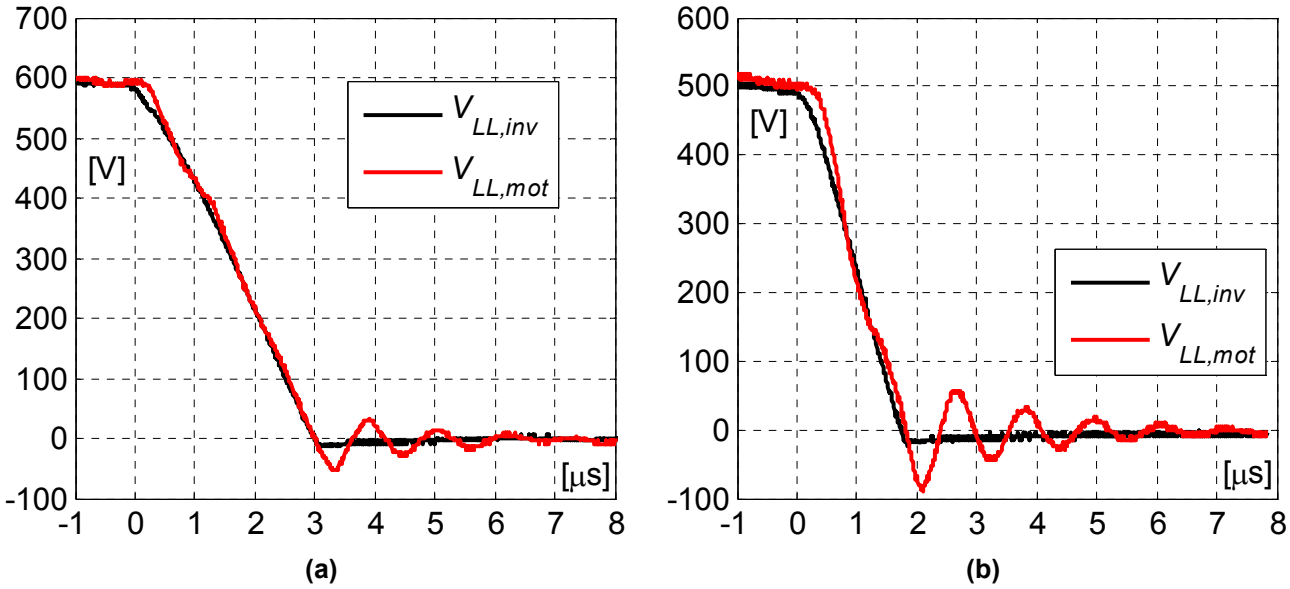


Figure 4.7 Line to line voltage at inverter and motor terminals (a) no load (b) with load

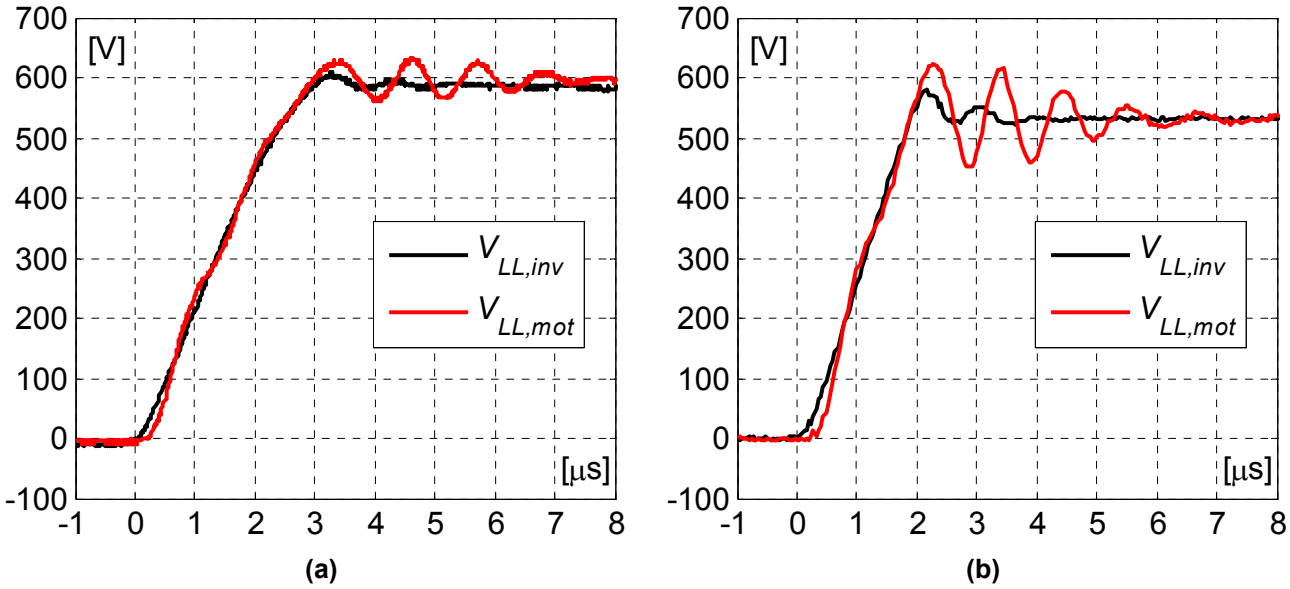


Figure 4.8 Line to line voltage at inverter and motor terminals (a) no load (b) with load

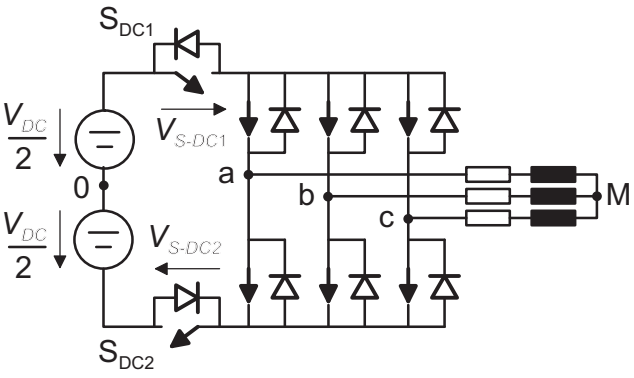


Figure 4.9 Simplified circuit for common mode voltage calculation

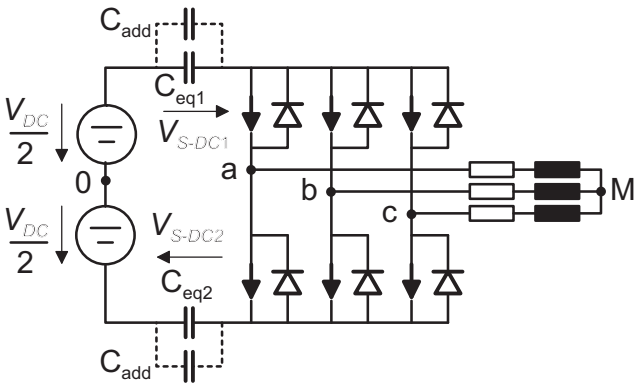


Figure 4.10 Simplified circuit with equivalent and added capacitances

4.5 Common mode voltage

As discussed in the section 2.4.1, the common mode voltage in QRDCL inverter can be reduced by adding an additional switch to the resonant circuit (Figure 4.9). The switches S_{DC1} and S_{DC2} together helps in completely separating Inverter Bridge from DC-link and this leads to an elimination of common mode voltage during the time interval of the zero voltage vectors ($\vec{V}_{07}$).
The analytical expression for the common mode voltage is

$$V_{M0} = \frac{V_{a0} + V_{b0} + V_{c0}}{3} \tag{4.1}$$

where V_{a0}, V_{b0} and V_{c0} are the voltages between inverter output phases and inverter DC midpoint. The hard switching inverter has three switches conducting at any given time corresponding to eight switching states. Then the instantaneous common mode voltage results in [13]:

$$V_{M0} = \begin{cases} \pm\frac{V_{DC}}{2} & \text{all top or bottom switches are on} \\ \pm\frac{V_{DC}}{6} & \text{one top and two bottom switches are on or viceversa} \end{cases} \tag{4.2}$$

The zero vector leads to the voltage vector of zero magnitude. The zero voltage vector in hard switching inverter is implemented either by turning on all the top switches ($\vec{V}_7$) or bottom switches ($\vec{V}_0$). The zero voltage vector in selected QRDCL inverter is implemented by turning on all the inverter switches ($\vec{V}_{07}$). The phase voltages during zero vector are:

$$V_{aM} = V_{bM} = V_{cM} = 0 \tag{4.3}$$

The zero voltage vector ($\vec{V}_{07}$) is the resonant cycle zero voltage period and during this time the switches S_{DC1} and S_{DC2} are open. If the switches S_{DC1} and S_{DC2} share the voltage equally, then the voltage across the switches is given by the following equation:

$$V_{S-DC1} = V_{S-DC2} = \frac{V_{DC}}{2} \tag{4.4}$$

From Figure 4.9, the common mode voltage can be expressed as:

$$V_{M0} = \frac{V_{DC}}{2} - V_{S-DC1} - V_{aM} \tag{4.5}$$

$$V_{M0} = -\frac{V_{DC}}{2} + V_{S-DC2} - V_{aM} \tag{4.6}$$

From (4.3), (4.4), (4.5) and (4.6), the common mode voltage during zero voltage vector is

$$V_{M0} = 0 \tag{4.7}$$

In the resonant inverter, the common mode voltage during zero voltage period is reduced from $\pm V_{DC}$ /2 to 0. This is valid only when the switches share the voltage equally. Under real circumstances, it is observed that the switches have the unequal voltage sharing (Figure 4.11).

The switches have stray capacitances in parallel and can be represented as shown in Figure 4.10. During turn-off, MOSFETs possess stray capacitances between drain and source. This capacitance together with the other stray capacitances to ground of the entire system, they build the equivalent capacitances between drain and source. These capacitances have different values depending upon the previous and next PWM states. When the resonant cycle follows the positive V_{M0}, i.e. previous PWM state 110 (where 1 is upper switch closed, 0 is lower switch closed), the voltage shared by the equivalent capacitances is:

$$V_{S-DC1} \approx \frac{V_{DC}}{3}, \quad V_{S-DC2} \approx \frac{2V_{DC}}{3} \tag{4.8}$$

Then the equivalent capacitances are in the ratio of

$$C_{eq1} \approx 2C_{eq2} \tag{4.9}$$

When the resonant cycle follows the negative V_{M0}, i.e. previous PWM state 100 (where 1 is upper switch closed, 0 is lower switch closed), the voltage shared by the equivalent capacitances is:

$$V_{S-DC1} \approx \frac{2V_{DC}}{3}, \quad V_{S-DC2} \approx \frac{V_{DC}}{3} \tag{4.10}$$

Then the equivalent capacitances are in the ratio of

$$C_{eq2} \approx 2C_{eq1} \tag{4.11}$$

The unequal capacitance's effect can be compensated by placing a large parallel capacitor (C_{add}) across each MOSFET, as shown in Figure 4.10. The switches S_{DC1} and S_{DC2} turn on and off at zero voltages. So a parallel capacitor will not produce any additional turn on losses in the MOSFETs. But very large capacitors will give the oscillations in $V_{S\text{-}DC1}$ and $V_{S\text{-}DC2}$ transients, which will finally lead to increase of oscillations in Inverter Bridge input voltage. So an optimal value of C_{add} = 15 nF is found empirically for the considered inverter cable with RL load.

The voltage sharing with the additional capacitor and RL load are shown in Figure 4.12. But this added capacitance is not sufficient for the inverter cable with motor load due to the motor stray capacitance to ground. The effect of increased system's ground stray capacitance, with motor load, brings higher oscillations in common mode voltage and is observed in Figure 4.13 and Figure 4.14. Measurement show that even C_{add} = 22 nF is not sufficient (Figure 4.13). Only a value C_{add} = 33 nF leads to significant improvement in voltage sharing across the DC-link switches (Figure 4.14).

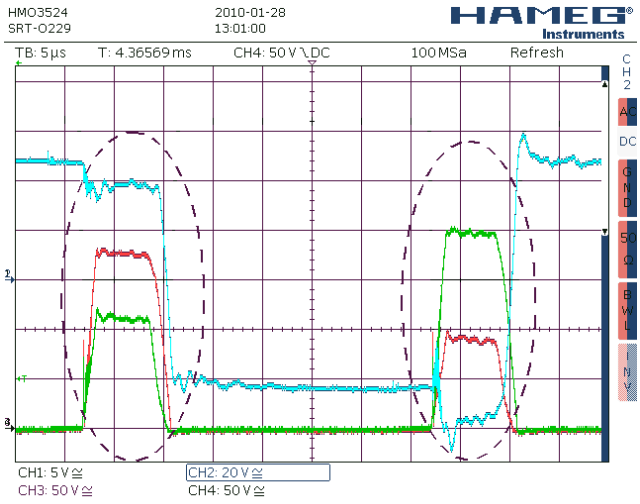


Figure 4.11 Voltage sharing with RL-passive load connection (C_{add} = 0 nF)

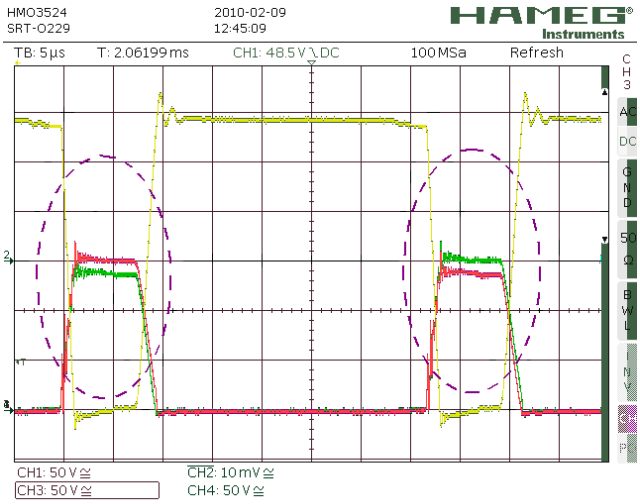


Figure 4.12 Voltage sharing with RL-passive load connection (C_{add} = 15 nF)

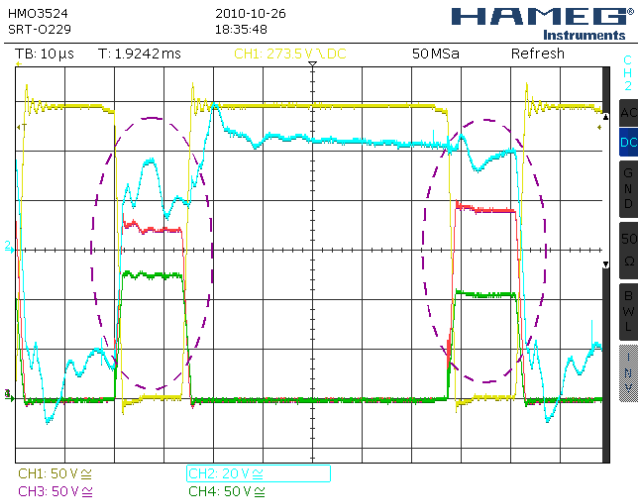


Figure 4.13 Voltage sharing with motor load connection (C_{add} = 22 nF)

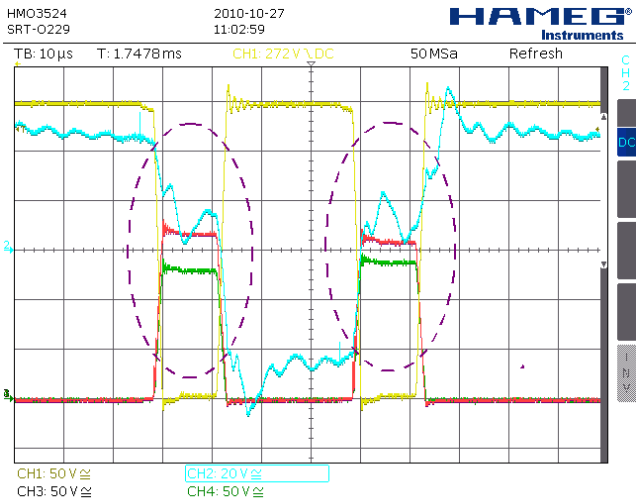


Figure 4.14 Voltage sharing with motor load connection (C_{add} = 33 nF)

Legend: Voltage on S_{DC1} ($V_{S\text{-}DC1}$): 50V/div (**Green**); Voltage on S_{DC2} ($V_{S\text{-}DC2}$): 50V/div (**red**); CM voltage (V_{M0}): 20V/div (**blue**); Voltage across inverter bridge (V_C): 50V/div (**yellow**).

4.6 Motor friendly characteristics

In order to evaluate the motor friendly characteristics of QRDCL inverter, the experimental results regarding the line to line voltage and line to earth voltage are taken at both ends of the long cable. Additionally, the common mode voltage is measured. To appreciate the performance of QRDCL inverter, the measurements are also taken for HS inverter with and without filters. Here, the common mode voltage is measured across the neutral point of the load and DC-link midpoint.

- **Hard switching inverter + 34m Long cable + No filter** (Figure 4.15): Over voltage at the motor side due to the high *dv/dt* and long cable can be observed. The oscillation period depends upon the cable stray elements. Similar oscillations can be observed in line to earth voltage also. The common mode voltage has higher harmonics due to the long

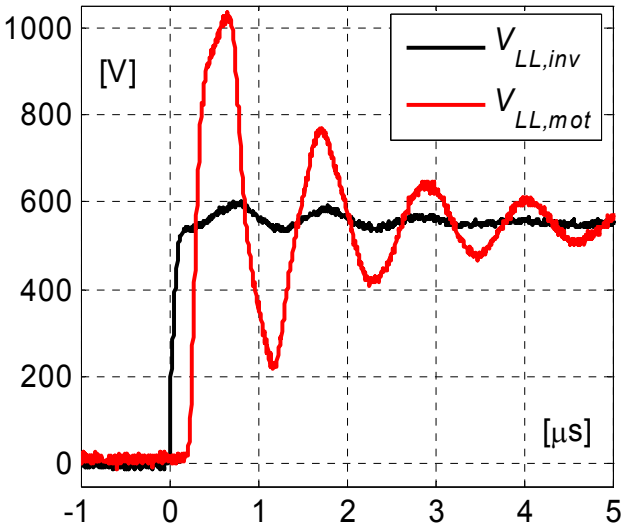
cable. Because of the high *dv/dt* in CM voltage, there will be a significant amount of leakage current through the capacitive coupling of stray capacitances.

- **Hard switching inverter + 34m Long cable + *dv/dt* filter** (Figure 4.16): The *dv/dt* filter increases the rise time of a line to line voltage and thereby voltage peaks at the motor are reduced, when compare to the previous case. The frequency of the ringing oscillations is also reduced. This filter has nearly no effect on the peak of common mode voltage.

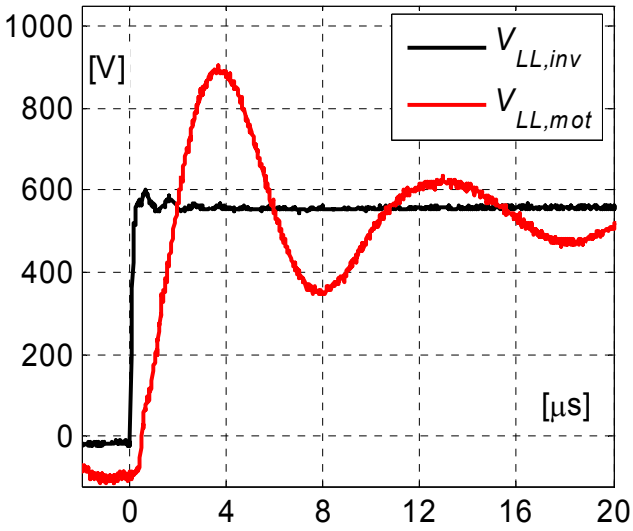
- **Hard switching inverter + 34m Long cable + Sine wave EMC filter** (Figure 4.17): A near sinusoidal line to line voltage waveform can be observed at the motor side. Thus no high *dv/dt*, and voltage stress on the motor has been eliminated. The line to earth voltage at motor terminals is free of high frequencies. The CM voltage has smaller oscillations only during the PWM commutation. The ringing oscillations are completely eliminated.

- **Soft switching inverter + 34m Long cable + No filter** (Figure 4.18): The soft switching inverter is designed for maximum voltage gradient of 600 V/µs. So the reduced *dv/dt* almost eliminates the ringing effect in the long cable. The reduced voltage reflections at the motor terminal can be observed. The CM voltage and line to earth voltage have a similar waveform. The oscillations in line to earth voltage are completely eliminated. Due to the zero vector implementation within the resonant cycle, the levels of the common mode voltage are limited to within ± 100 V. The slope of the common voltage is also reduced causing very low leakage currents.

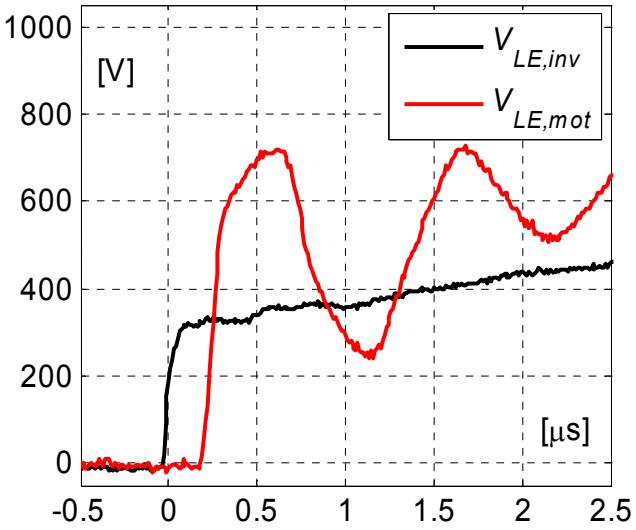
The performance of the SS inverter is comparable to HS inverter with a sine-wave EMC filter. For the HS inverter, the use of a filter increases the cost and weight of the power converters. The current sensing at both inverter output and filter output is required. The motor-friendly soft switching inverter does not need an output filter. So it has good dynamics compare to a hard switching inverter with a sine-wave EMC output filter. In summary, the comparative study based on experimental results suggests that motor-friendly SS inverter is an alternative to HS inverter with a sine-wave EMC output filter.



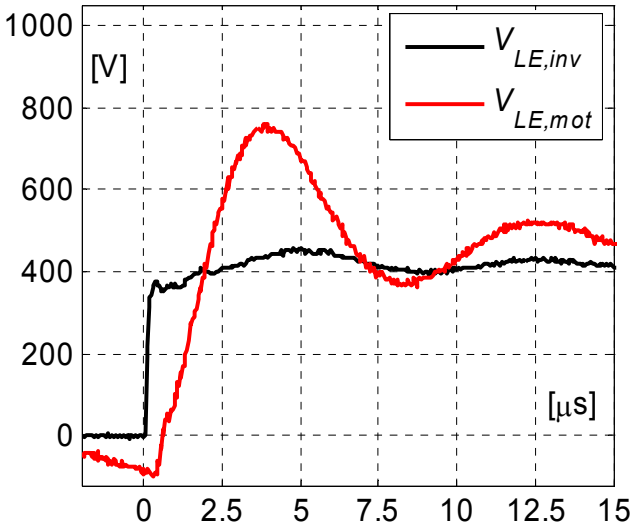
(a) Line to line voltage



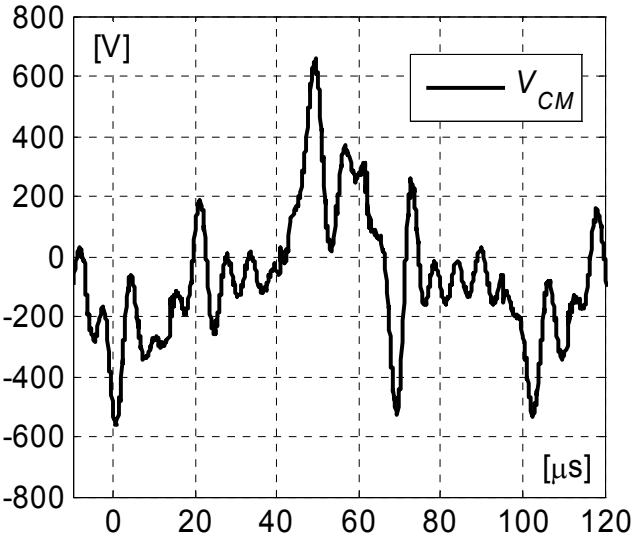
(a) Line to line voltage



(b) Line to earth voltage

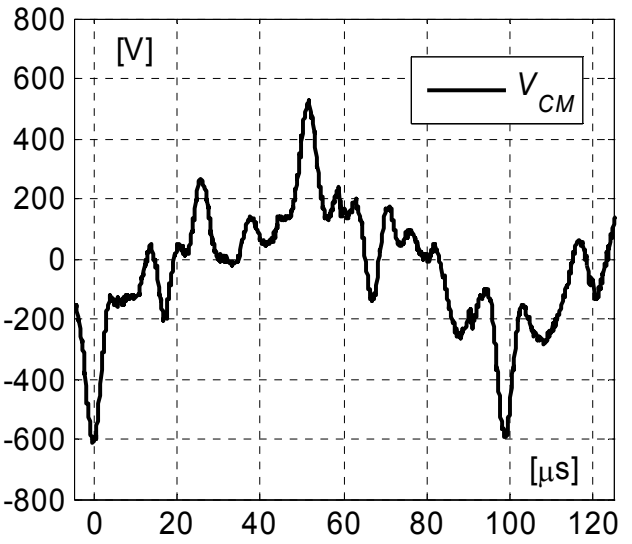


(b) Line to earth voltage



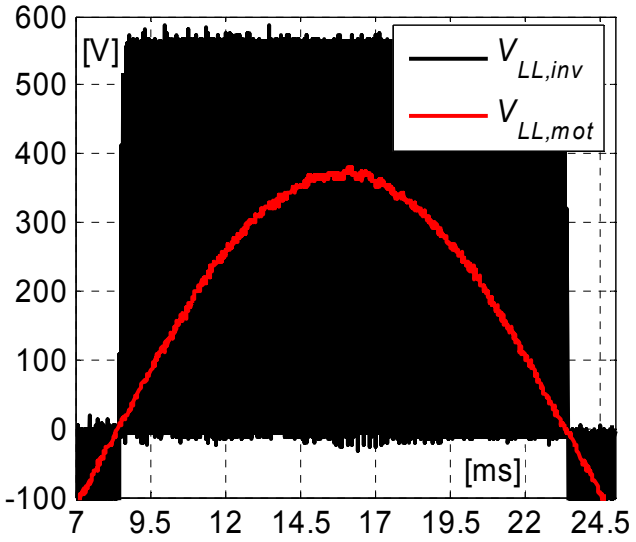
(c) Common mode voltage

Figure 4.15 HS inverter

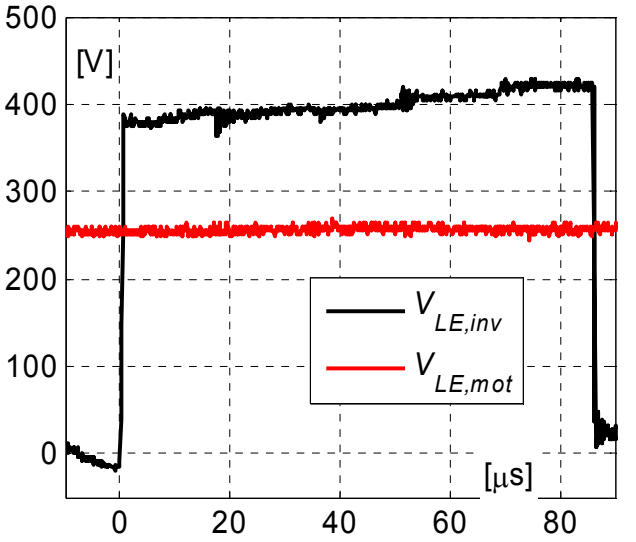


(d) Common mode voltage

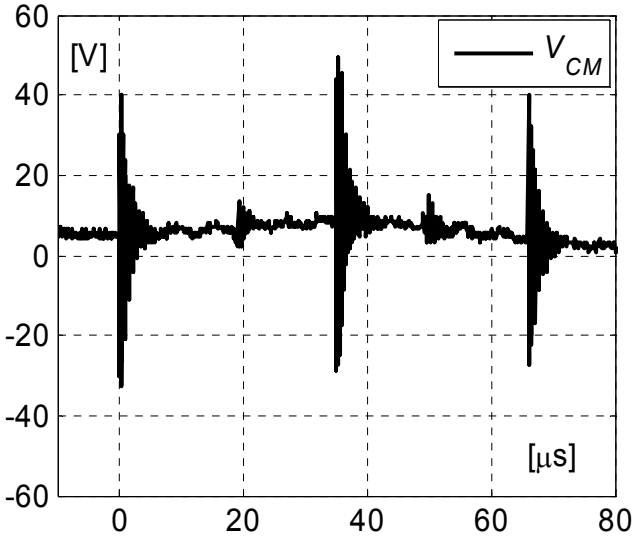
Figure 4.16 HS inverter with *dv/dt* filter



(a) Line to line voltage

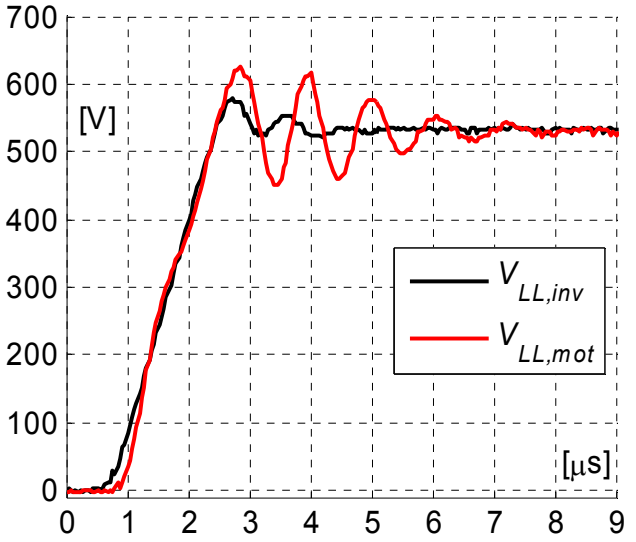


(b) Line to earth voltage

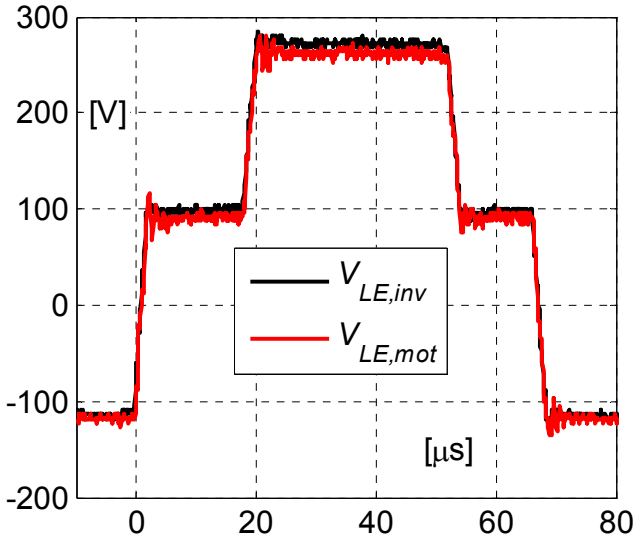


(c) Common mode voltage

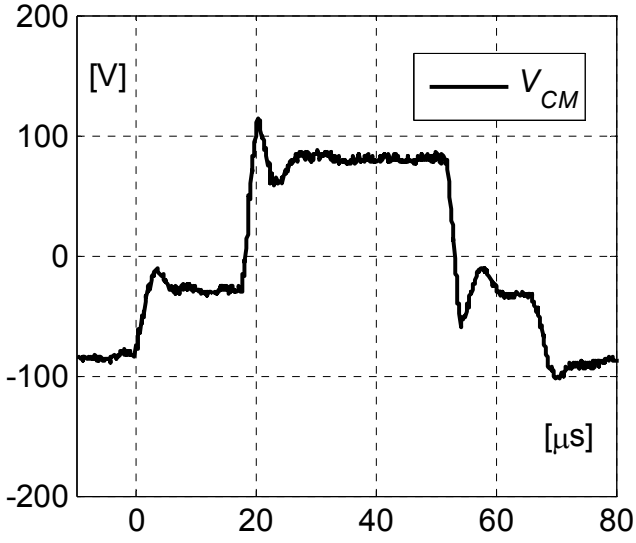
Figure 4.17 HS inverter with Sine wave EMC filter



(a) Line to line voltage



(b) Line to earth voltage



(c) Common mode voltage

Figure 4.18 SS Inverter

4.7 Indirect field oriented control

Using field oriented control techniques, the flux and torque can be controlled in a decoupled manner, yielding fast response in torque and speed control. The implementation of field oriented control in FPGA is presented in section 3.4. The response to a step in the speed reference (1000 rpm = 104.72 rad/s) is shown in Figure 4.19. It shows the measured speed (ω) at no load. The torque component current follows (i_q) the generated torque component reference current (i_{qref}). The flux component current (i_d) is maintained constant. Figure 4.20 shows the 3-phase motor line current wave forms. A sudden step change in the load torque from 0 to 10 Nm is applied at 3.15s (Figure 4.21). The q-axis current component is increased to generate the necessary torque. The speed is maintained constant by speed control and IFOC. In a similar way, the results for step change in the load torque from 0 to 15 Nm are shown in Figure 4.22.

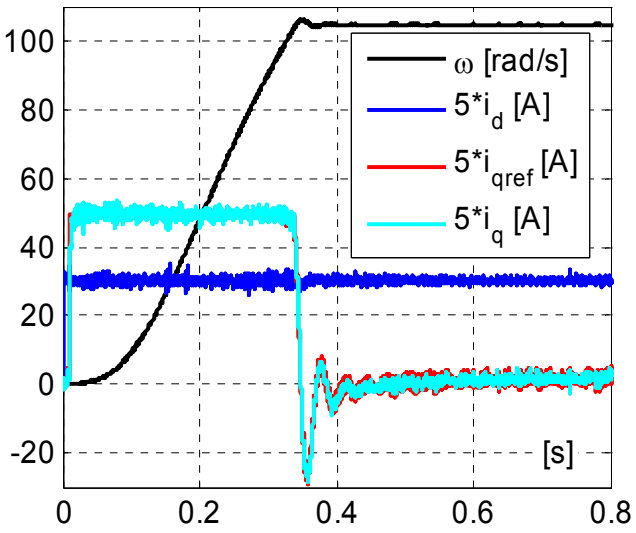


Figure 4.19 Speed, q-axis reference current, dq-axes currents for a step change in the Speed reference (from 0 to 104.72 rad/s)

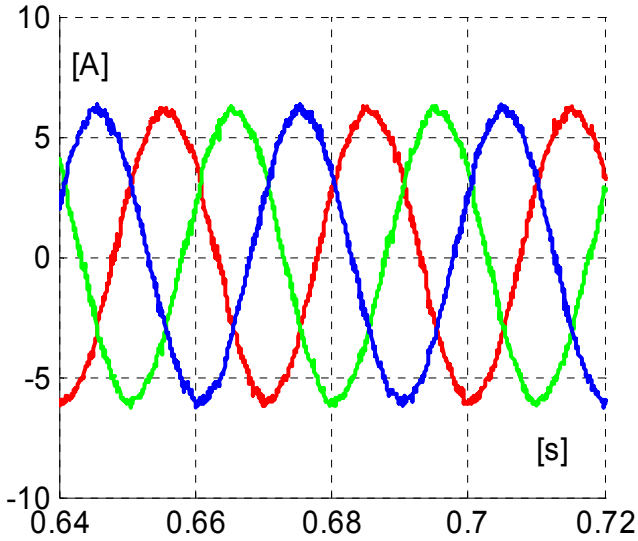


Figure 4.20 Motor line currents

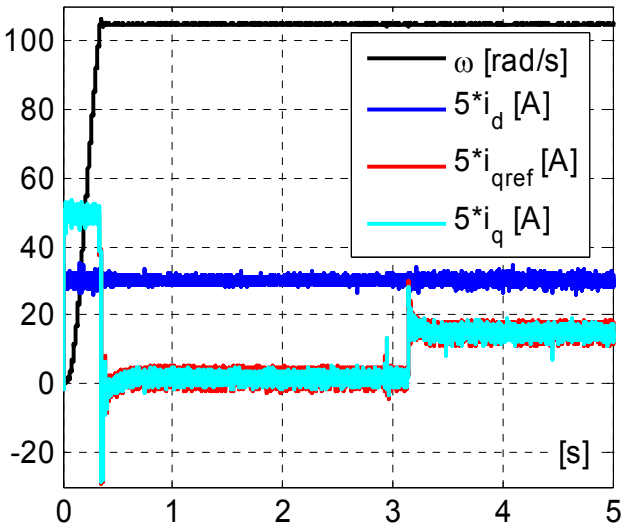


Figure 4.21 Speed, q-axis reference current, dq-axes currents for a step change in the load torque (from 0 to 10 Nm)

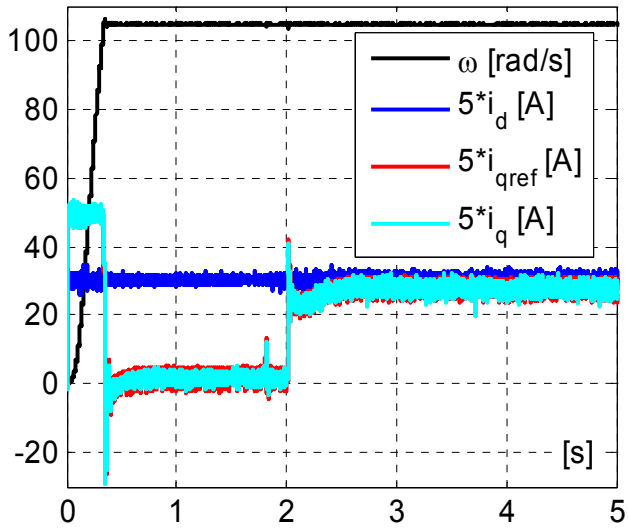


Figure 4.22 Speed, q-axis reference current, dq-axes currents for a step change in the load torque (from 0 to 15 Nm)

4.8 Efficiency measurements

The efficiency measurements are taken for the hard switching inverter with and without filters and for the soft switching inverter. For HS and SS modes of the inverter, voltage and current measuring points are displayed in Figure 4.23 and Figure 4.24 respectively. The efficiency for a fixed speed and a fixed load torque is measured by power meter. The speed of the induction machine is kept constant by IFOC implemented in FPGA. Then the load torque is controlled by controlling the armature current of a DC generator. The power meter NORMA 5000 is used to measure the efficiency. It has a very high bandwidth of 1MHz and 6 channels to measure the power. The efficiency measurements are presented for different speed and load torques. The total losses (inverter + filter, if any) are also presented for different speed and torques. The following notations are used in the figures:

- HS nF S: Hard switching inverter with no output filter and using short cable.
- HS nF: Hard switching inverter with no output filter and using long cable.
- HS *dv/dt*: Hard switching inverter with *dv/dt* filter and using long cable.
- HS SW: Hard switching inverter with sine wave EMC filter and using long cable.
- SS: Soft switching inverter with no output filter and using long cable.

The SS inverter is designed for the low voltage gradient at the inverter output. With the help of an additional switch (S_{DC2}) and the modified modulation, the common mode voltage is also reduced. During the voltage falling and voltage rising time, the resonant elements supply the load current. With an increase in the rise and fall time, the energy needed to be stored in the resonant inductor also increases. So the losses in the SS inverter rise. The extended resonant cycle causes freewheeling of the inductor current through the inverter switches resulting in more losses. So the efficiency of a SS inverter simply cannot be compared with a HS inverter alone.

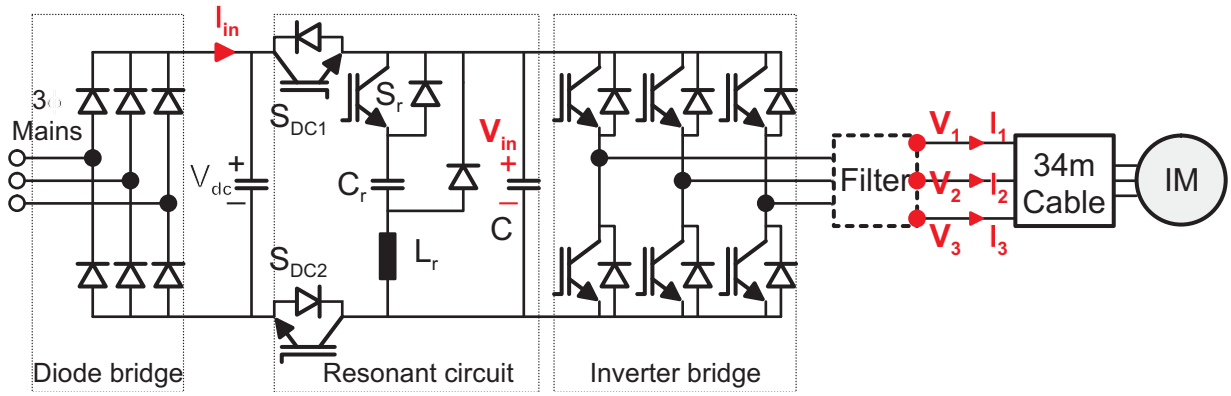


Figure 4.23 Hard switching inverter mode

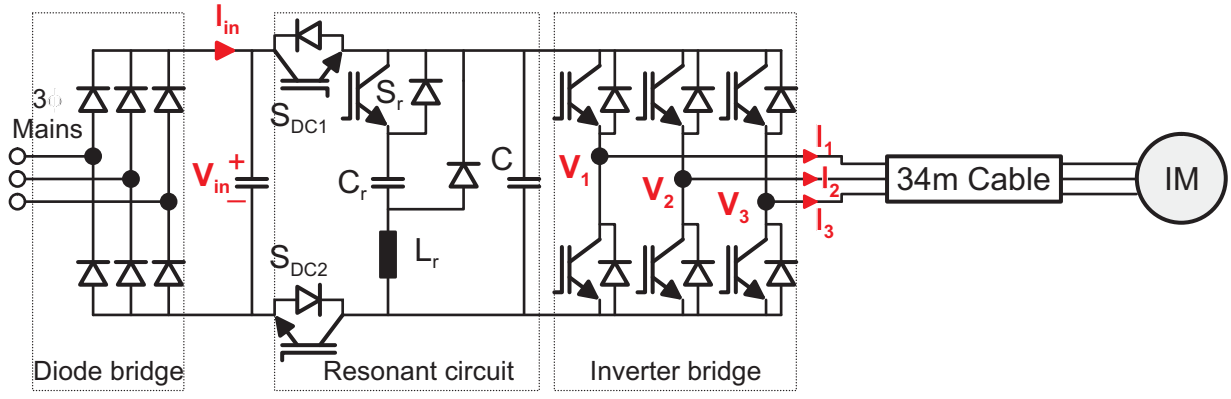


Figure 4.24 Soft switching inverter mode

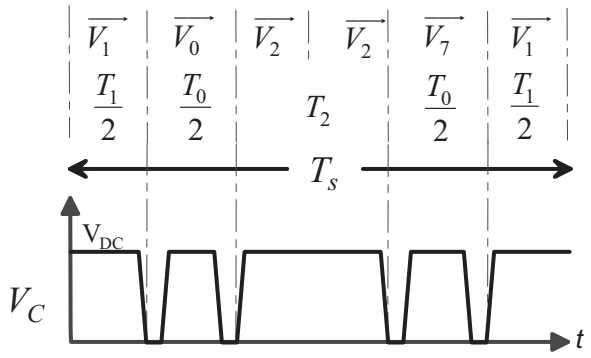


Figure 4.25 Short resonant cycles

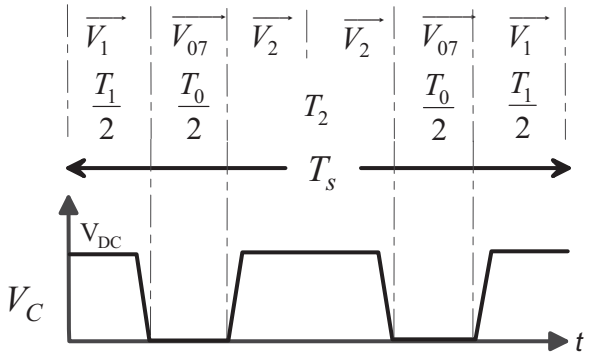


Figure 4.26 Extended resonant cycles

➢ **SS inverter for *dv/dt* reduction only**: Here, the SS inverter operates only for the *dv/dt* reduction. The modulation technique implemented is shown in Figure 4.25. Indeed, the extended resonant cycle discussed in section 2.4.1 for the CM voltage reduction is not required. Before every switching, the resonant cycle is implemented. So the modified modulation requires for 4 resonant cycles in one switching period. The increase in the number of resonant cycle increases the losses and also decreases the available modulation index. So the modulation is modified such that,

- If the zero vector time (T_0/2) > 20 µs, two resonant cycles occurs between the two active vectors $\vec{V}_1$ and $\vec{V}_2$ (Figure 4.25).
- If the zero vector time (T_0/2) < 20 µs, the extended resonant cycle takes place between the two active vectors $\vec{V}_1$ and $\vec{V}_2$ (Figure 4.26). This usually occurs at high modulation indexes and middle of the sectors.

Overall, the SS inverter performs a *dv/dt* filtering. Figure 4.29 shows the efficiency of a SS inverter and HS inverter with *dv/dt* filter and sine wave EMC filter. The results indicate the SS inverter has higher efficiency compared to HS inverter with a *dv/dt* filter. The SS in *dv/dt* filter mode has almost the same efficiency as HS inverter with a sine wave EMC filter. The importance of this comparison is explained later in this chapter.

The efficiency of HS inverter with a sine wave EMC filter is higher than with a *dv/dt* filter. Even though the losses are higher for sine-wave filter (Figure 4.31b) than *dv/dt* filter (Figure 4.32b), overall losses of HS inverter with a sine-wave filter are lower than HS inverter with a *dv/dt* filter. The lower current ripple in case of using sine-wave filter i.e. lower RMS value of current reducing the conduction losses in the inverter semiconductors. This is explained by the fact, that the sine wave filter reduces the current ripple which intern reduces the RMS value of the current. The reduced RMS value causes reduced conduction losses in the inverter. This reduction of conduction losses is greater than the increase of losses due to the change from *dv/dt* filter to the sine-wave filter.

➢ **SS inverter for *dv/dt* and CM voltage reduction**: Here, the SS inverter reduces the *dv/dt* and also CM voltage level. So, the extended resonant cycle discussed in section 2.4.1 for CM voltage reduction is used. During the zero voltage period, high inductor current is freewheeling for longer time causing the increase in temperature of the relatively thin copper layer of the PCB used in the experimental set-up. The modulation technique is modified to avoid the longer resonant cycles.

- If the zero vector time t_Z < 50 µs, the extended resonant cycle takes place between the two active vectors. (Figure 4.27).
- If the zero vector time t_Z > 50 µs, two resonant cycles occurs between the two active vectors (Figure 4.28). This usually occurs at low modulation indexes.

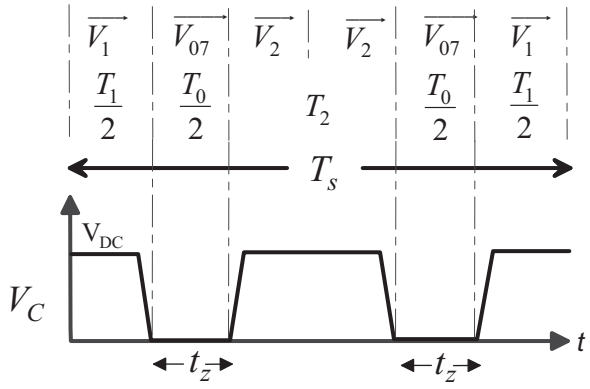


Figure 4.27 Extended resonant cycles

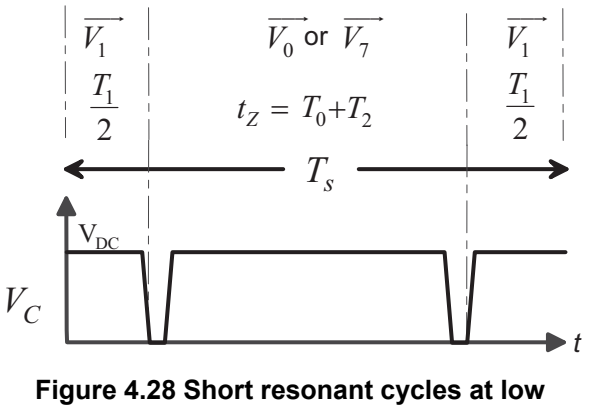
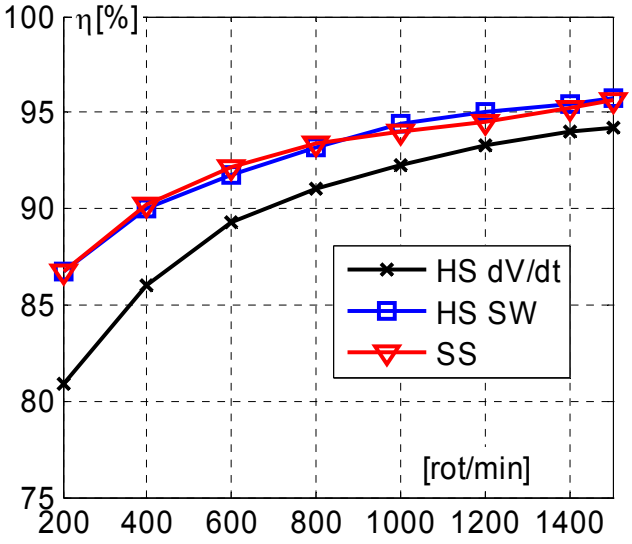


Figure 4.28 Short resonant cycles at low modulation index

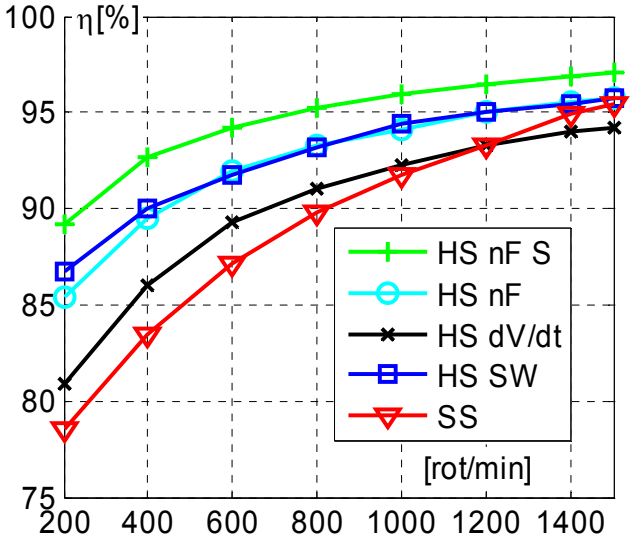
At very low modulation indexes, this modulation of the SS inverter is not reducing the common mode voltage. This limitation can be overcome by a thicker copper layer of the PCB. From Figure 4.30, it can be concluded that HS inverter with a sine-wave EMC filter has higher efficiency compare to SS inverter. The difference in the efficiencies is very small at higher modulation indexes, i.e. at higher output power. With the decrease in the speed, the efficiency of SS inverter is decreasing rapidly.

For a motor-friendly characteristic, the zero vector time is included in the resonant cycle. However, it is reducing the efficient characteristic of the SS inverter. In SS inverter, the zero voltage period of time is extended and the inductor current free wheels through a diode and inverter switches. The freewheeling inductor current is gradually reduced by the voltage drops of line resistance, diode and inverter switches. The considerable part of stored energy in the inductor is wasted as conduction losses. So the level of the trip current is increased otherwise the inverter input voltage will not reach the DC-link source voltage. The increase in a trip current and freewheeling inductor current produces substantial losses in the inverter. For low modulation index, a longer zero voltage period is needed. The losses during the freewheeling period are very high and the efficiency of the inverter is reduced to a low value.

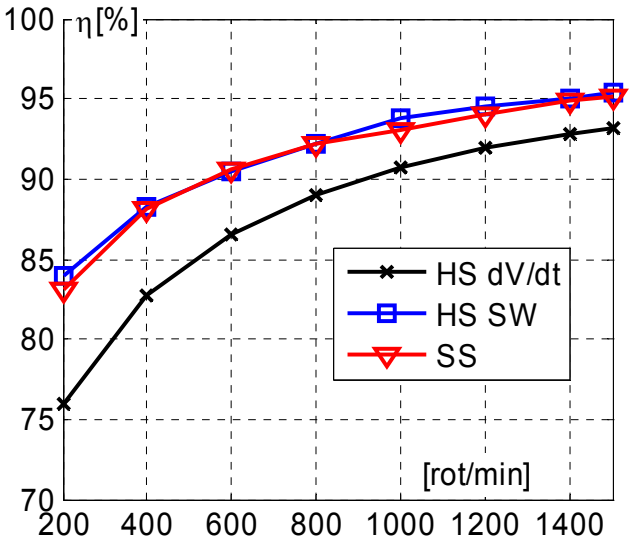
The efficiency plots for various speeds and load torques are shown in Figure 4.30. The different losses in the inverter, filter and resonant inductor are given in Figure 4.31, Figure 4.32, Figure 4.33 and Figure 4.34. Hard switching inverter without any filter and short cable connected between inverter and motor has higher efficiency above all the other. But with long cable connected, the inverter has low efficiency because of high ripple current loading the capacitance of the cable. The sinusoidal filter eliminates the pulse reflections in the motor cable and there by reduces the losses in the inverter [17]. In Figure 4.29, SS inverter efficiency is equal to of HS inverter with a sine-wave EMC filter. In Figure 4.30, SS inverter efficiency is less than that of HS inverter with a sine-wave EMC filter. Here, the resonant cycles with longer zero voltage durations are producing high losses in the SS inverter. In order to improve the efficiency of the inverter, a SS inverter with a loss less variable zero voltage duration is required. Then SS inverter will have same efficiency as HS inverter with a sine-wave EMC filter.



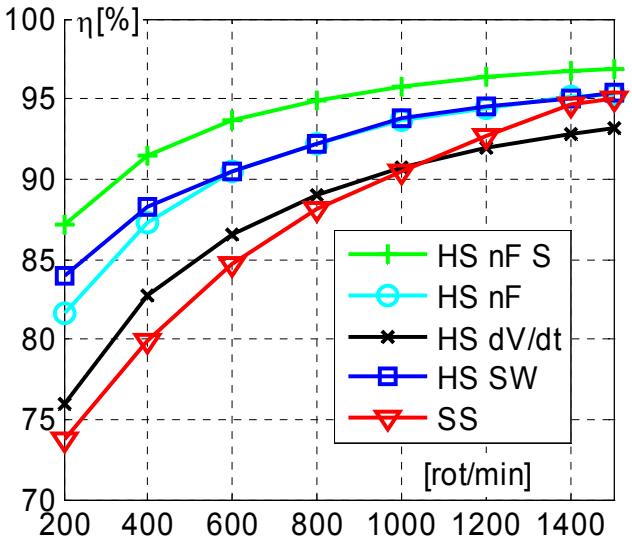
Efficiency plot (T = 20 Nm)



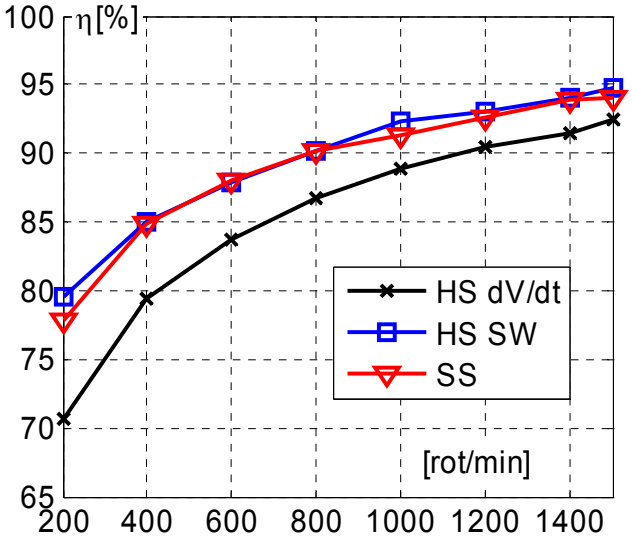
Efficiency plot (T = 20 Nm)



Efficiency plot (T = 15 Nm)

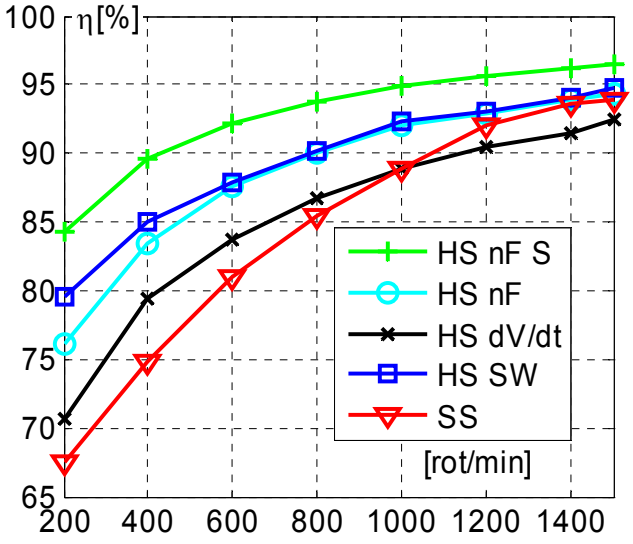


Efficiency plot (T = 15 Nm)



Efficiency plot (T = 10 Nm)

Figure 4.29 Efficiency comparison (Soft switching inverter reducing only *dv/dt*)



Efficiency plot (T = 10 Nm)

Figure 4.30 Efficiency comparison (Soft switching inverter reducing *dv/dt* and CMV)

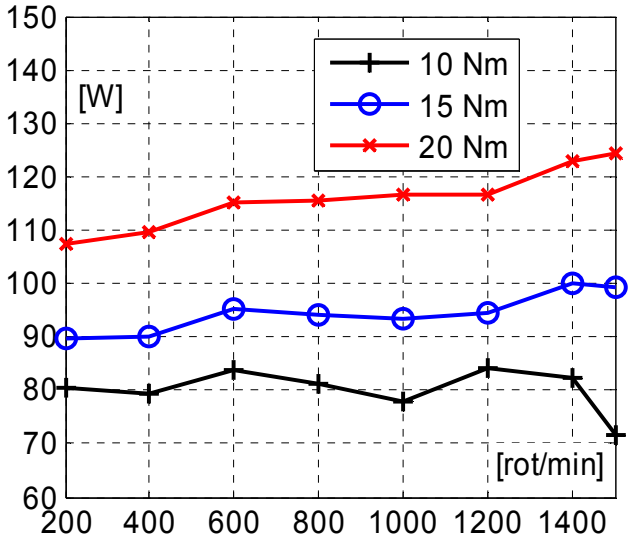
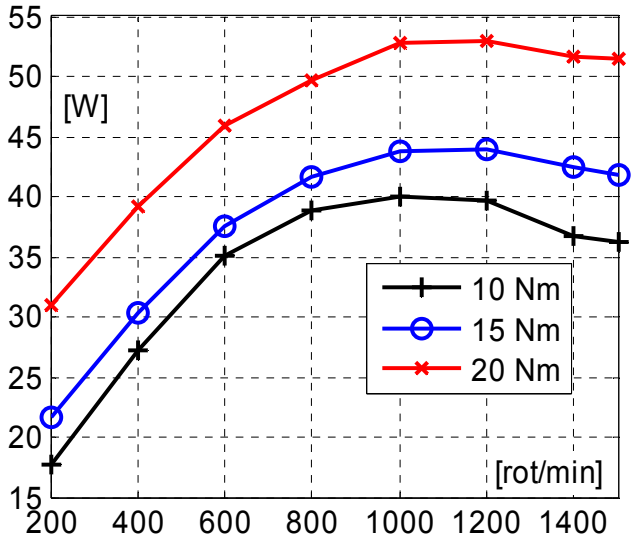


Figure 4.31 HS SW: (a) Losses in inverter



(b) Losses in filter

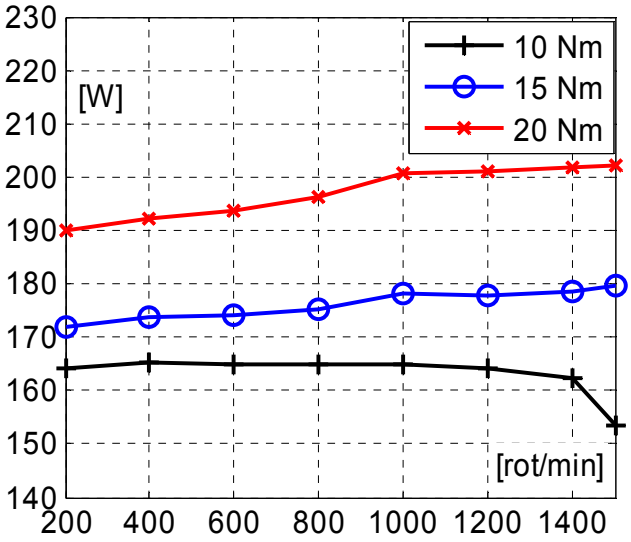
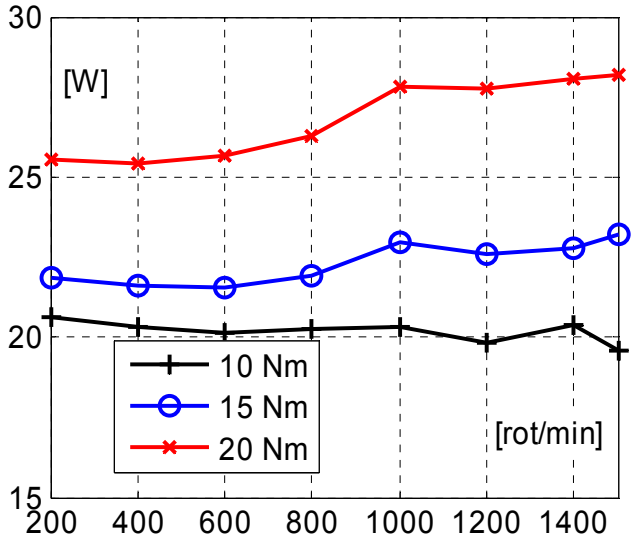


Figure 4.32 HS *dv/dt*: (a) Losses in inverter



(b) Losses in filter

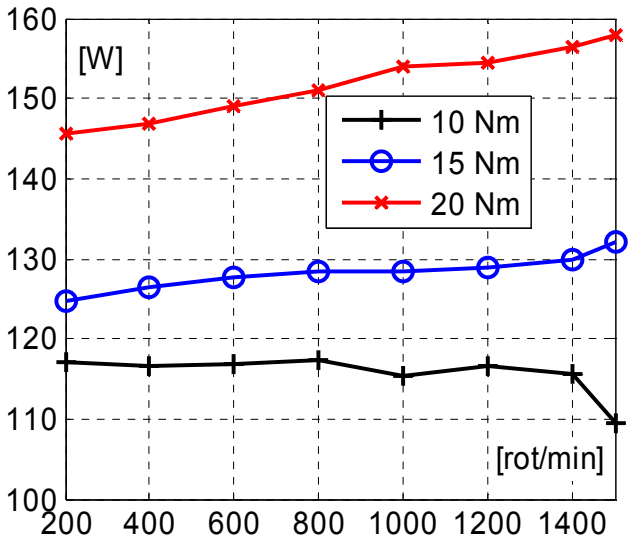


Figure 4.33 HS nF: Total losses

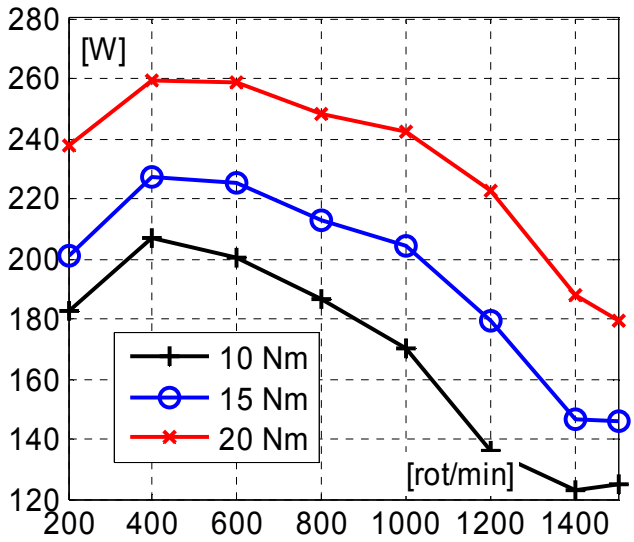


Figure 4.34 SS: Total losses

4.9 Conclusions

The soft switching inverter is designed to be motor friendly. In this chapter, the reduction of high frequency parasitic effects is tested. The efficiency of the QRDCL inverter is measured. The efficiency of a hard switching inverter with filters is also measured for comparison. The SS inverter alone has much higher efficiency when compare to the HS inverter with a *dv/dt* filter. But the SS inverter has lower efficiency when compare to the HS inverter with a sine wave EMC filter. It is concluded that SS inverter with a loss less zero variable zero voltage duration will have equal efficiency as with a sine wave EMC filter. The efficiency of a resonant DC-link converter can be improved further by use of new semiconductor technology optimised for low switching and conduction losses. In summary, the comparative study based on experimental results suggests that motor-friendly SS inverter is an alternative to HS inverter with a sine-wave EMC output filter.

5 A Novel Quasi-resonant DC-Link Inverter with Lossless Variable Zero Voltage Duration

5.1 Introduction

As discussed previously, to reduce the common mode voltage level during zero vector time, the inverter is completely separated from DC-link. For the motor friendly characteristic, zero vector time is included in a resonant cycle. However, it is reducing the efficient characteristic of the inverter. In topology T2, the zero voltage period of time is extended and the inductor current free wheels through a diode and inverter switches. The freewheeling inductor current is gradually reduced by the voltage drops of line resistance, diode and inverter switches. The considerable part of stored energy in the inductor is wasted as conduction losses. So the level of the trip current is increased otherwise the inverter input voltage will not reach the DC-link source voltage. The increase in a trip current and freewheeling inductor current produces substantial losses in the inverter. For low modulation index, a longer zero voltage period is needed. The losses during the freewheeling period are very high, and efficiency of the inverter is reduced to very low value. These effects are observed in the last chapter. So a lossless variable zero voltage duration is necessary for high efficiency of the QRDCL inverter.

A quasi resonant DC-link inverter with lossless variable zero voltage duration is presented in [77] and is shown in Figure 5.1. An additional switch can be added to the negative DC-link, so that complete separation of the inverter from DC-link is possible. But the upper and lower DC-link switches should be controlled separately. These switches turn off at different times. So a 650 V voltage blocking CoolMOS™ cannot be used. The lower DC-link switch conducts all the time during a resonant cycle except during the extended zero voltage period and thereby producing conduction losses. Moreover, this switch turns off and on at half of the DC-link voltage. The other disadvantage is that a connection to the DC-link mid-point is necessary. The added lower DC-link switch can be opened only when the inductor current is zero. So, for some time during mode M3, the CM voltage is not zero, but $-V_{dc}/2$. In conclusion, this circuit cannot be adopted for motor friendly application to reduce the CM voltage. However, in a positive way, the circuit is providing an idea of lossless variable zero voltage duration. It is adapted to topology T2 and a new QRDCL inverter is proposed.

A novel quasi-resonant DC-link inverter with lossless variable zero voltage duration is introduced in this chapter. This inverter works in similar fashion as of topology T2 except during the zero voltage period. The design procedure and the derivation of trip current are exactly same as for topology T2. They are discussed thoroughly in chapter 2 and are not repeated in this chapter. The control requirements are also same for both topologies. The proposed QRDCL inverter operation is discussed in detail here.

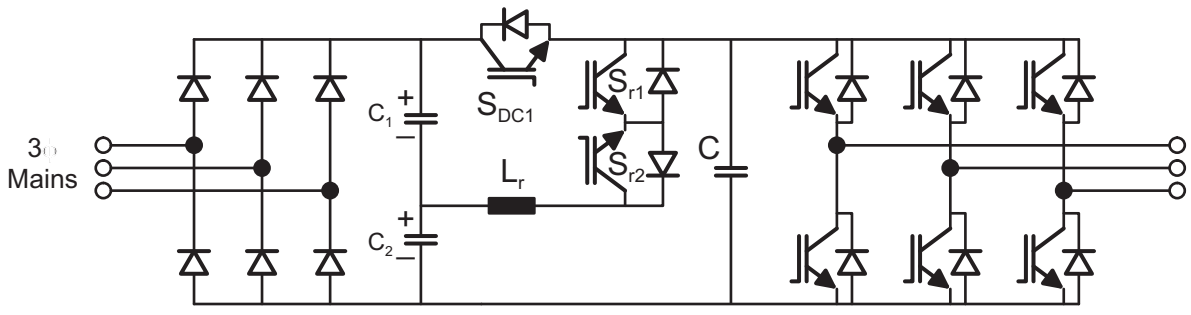


Figure 5.1 Quasi-resonant topology from [77]

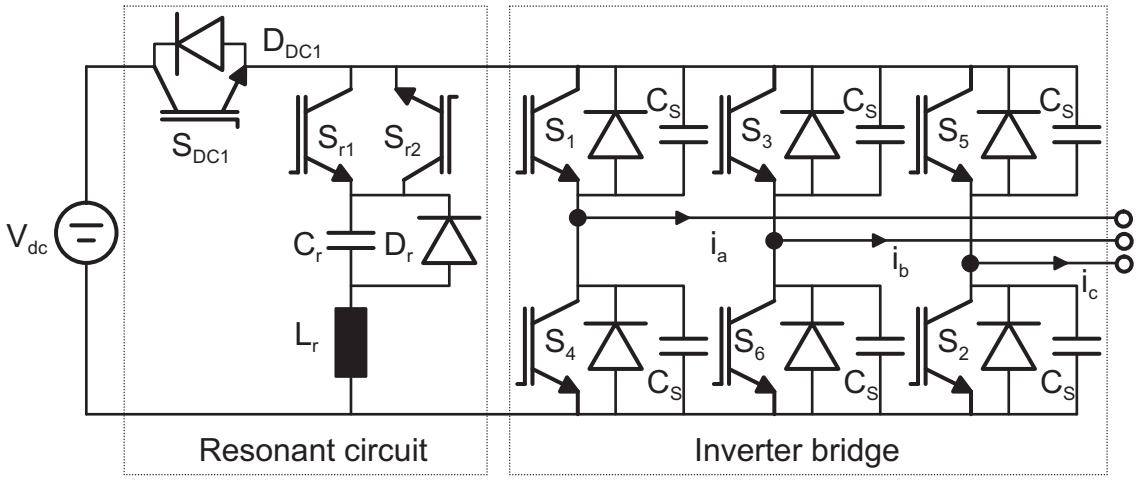


Figure 5.2 Circuit diagram of proposed Quasi-resonant DC-link inverter

The control of the resonant converter is little different to topology T2. The modified control is explained in this chapter. Simulation results are presented to validate the theoretical results.

5.2 Quasi-resonant DC-link Inverter (Topology T3)

Figure 5.2 shows a new quasi-resonant dc link inverter. It will be further called topology "T3". The lossless variable zero voltage duration is accomplished by only controlling the switch S_{r2}. The proposed resonant circuit consists of three additional switches, passive elements L_r, C_r and C_S. The resonant switches S_{r1} and S_{r2} are the reverse blocking anti-parallel IGBTs. The energy of the resonant circuit is zero in the steady state. In order to analyze the QRDCL inverter, the resonant circuit different modes are discussed here. To simplify the descriptions of operations of this circuit, the assumptions given in section 2.2 are also valid here.

For a switching period, the simplified equivalent circuit is as shown in Figure 5.3a. The resonant capacitor C is equal to $3C_S$. The related operational waveforms are shown Figure 5.3b and the different operating modes in Figure 5.4. The six switches of the bridge are represented by a single switch S_{INV} for the purpose of the analysis. The equivalent current source I_O represents the inverter's DC-link current whose value and direction depend on the individual phase currents of the machine and the status of inverter switches [39], [40].

This resonant circuit operation is similar to the resonant circuit (Topology T2) discussed in section 2.3. The difference comes only during a zero voltage period. So the equations for all the other modes will be same for both the topologies. For topology T2, the resonant energy is stored in a resonant inductor L_r and for topology T3, the resonant energy is stored in a resonant capacitor C_r. The topology T3 is discussed here in detail for each mode, and equivalent circuits are given in Figure 5.4.

The following notations are used in the subsequent equations:

$$C_{sum} = C + C_r,\ a = \frac{C_r}{C_{sum}},\ b = \frac{C}{C_{sum}},\ \omega_0 = \frac{1}{\sqrt{L_r C_r}},\ \omega_1 = \sqrt{\frac{C + C_r}{LCC_r}},\ \omega_2 = \frac{1}{\sqrt{L_r C}},$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}},\ Z_1 = \frac{1}{\omega_1 C},\ Z_2 = \omega_1 L,\ Z_3 = \frac{1}{\omega_1 C_r},\ Z_4 = \frac{1}{\omega_1 C_{sum}},\ Z_5 = \sqrt{\frac{L_r}{C}}$$

Mode M0 [t_0]**:** The resonant circuit is in the steady state. In the steady state, the resonant tank energy is zero, S_{DC1} is closed, S_{r1} and S_{r2} are open.

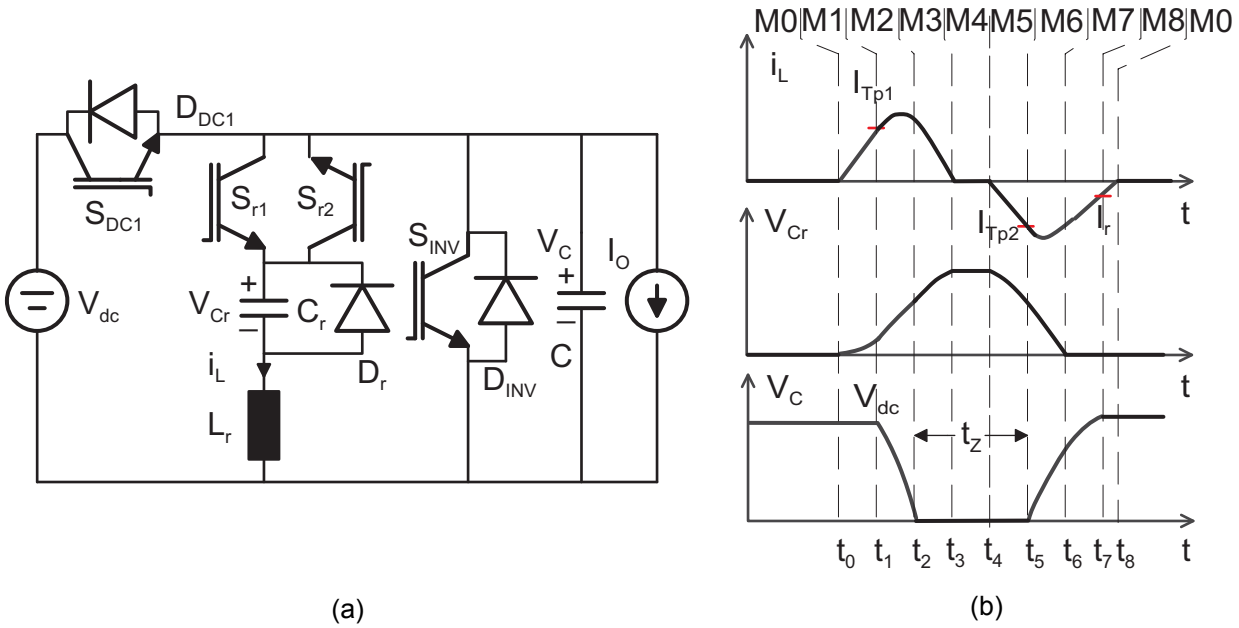


Figure 5.3 (a) Simplified circuit of new resonant converter (b) Typical waveforms

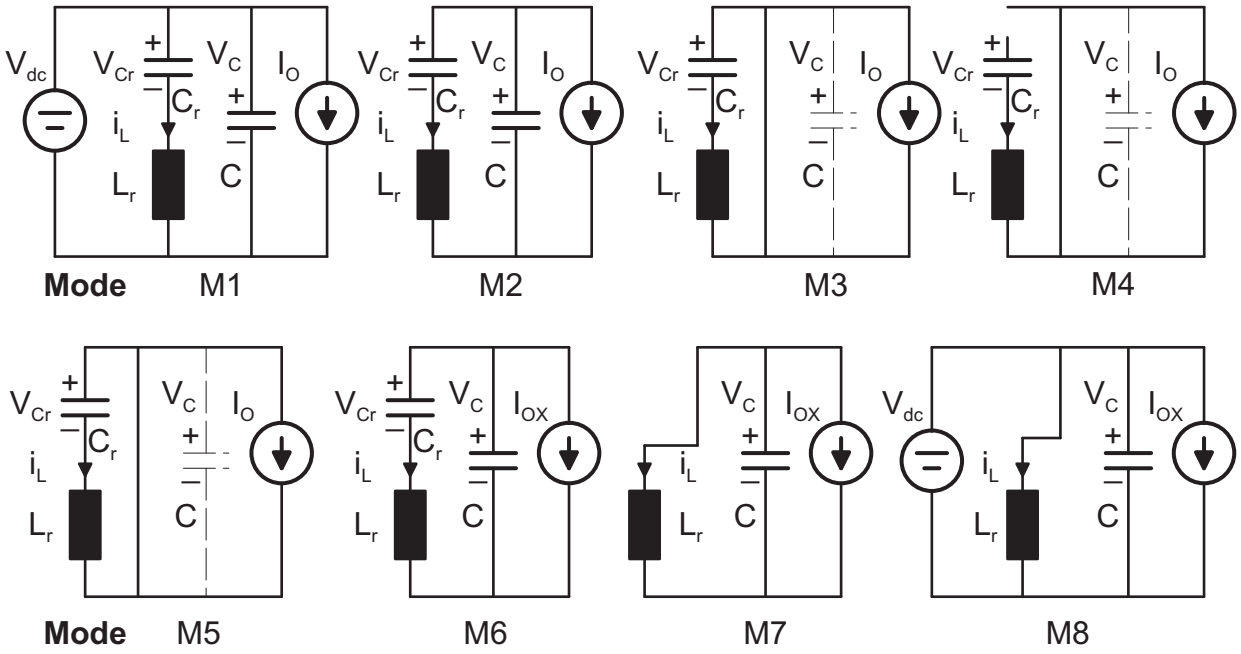


Figure 5.4 Operating modes during a resonant cycle

$$i_L(t_0) = 0 \tag{5.1}$$

$$V_{Cr}(t_0) = 0 \tag{5.2}$$

$$V_C(t_0) = V_{dc} \tag{5.3}$$

Mode M1 [t_0, t_1]**:** When a switching in PWM inverter is needed, the switch S_{r1} is turned on. Then the current i_L starts flowing through resonant elements L_r and C_r. Because the switch

S_{DC1} is closed, voltage across the inverter bridge (V_C) remains equal to DC-link voltage (V_{dc}). The energy needed to complete a resonant cycle is stored in resonant inductor L_r and resonant capacitor C_r.

$$\theta = \omega_0 (t - t_0)$$

$$i_L(t) = \frac{V_{dc}}{Z_0} \sin\theta \tag{5.4}$$

$$V_{Cr}(t) = V_{dc}(1 - \cos\theta) \tag{5.5}$$

$$V_C(t) = V_{dc} \tag{5.6}$$

$$\text{At } t = t_1, i_L(t_1) = I_{Tp1} \Rightarrow \sin\theta = \frac{I_{Tp1} Z_0}{V_{dc}} \Rightarrow \cos\theta = \frac{\sqrt{V_{dc}^2 - (I_{Tp1} Z_0)^2}}{V_{dc}} \tag{5.7}$$

$$\text{At } t = t_1, V_{Cr}(t_1) = V_{dc}(1 - \cos\theta) = V_{dc} - \sqrt{V_{dc}^2 - (I_{Tp1} Z_0)^2} \tag{5.8}$$

Mode M2 [t_1, t_2]**:** When the current i_L reaches the trip current level I_{Tp1}, the DC-link switch S_{DC1} is opened. Then the inverter bridge is separated from the DC-link, and voltage V_C decreases resonantly from V_{dc} to zero. The voltage falling time is decided by resonant elements and load current.

$$\theta = \omega_1 (t - t_1)$$

$$i_L(t) = (aI_O + i_L(t_1))\cos\theta + \frac{V_{dc} - V_{Cr}(t_1)}{Z_2} \sin\theta - aI_O \tag{5.9}$$

$$V_{Cr}(t) = b(V_{Cr}(t_1) - V_{dc})\cos\theta + Z_3(aI_O + i_L(t_1))\sin\theta + bV_{dc} + aV_{Cr}(t_1) - \frac{I_O(t - t_1)}{C_{sum}} \tag{5.10}$$

$$V_C(t) = a(V_{dc} - V_{Cr}(t_1))\cos\theta - Z_1(aI_O + i_L(t_1))\sin\theta + bV_{dc} + aV_{Cr}(t_1) - \frac{I_O(t - t_1)}{C_{sum}} \tag{5.11}$$

$$\text{At } t = t_2, V_C(t_2) = 0 \Rightarrow V_{Cr}(t_2) = \frac{Z_2}{Z_1}\left(V_{dc} - a\sqrt{V_{dc}^2 - (I_{Tp1} Z_0)^2} - \frac{I_O(t - t_1)}{C_{sum}}\right) \tag{5.12}$$

$$i_L(t_2) = \sqrt{\frac{V_{dc}^2 - (I_{Tp1} Z_0)^2}{Z_2^2} + (aI_O + i_L(t_1))^2 - \left(\frac{V_{Cr}(t_2)}{Z_2}\right)^2} - aI_O \tag{5.13}$$

Mode M3 [t_2, t_3]**:** When the DC-link voltage V_C reaches zero, all inverter switches are turned on. In terms of the simplified equivalent circuit, S_{INV} is turned on under zero voltage condition. So the voltage V_C remains zero. Due to resonance between C_r and L_r, the inductor current i_L reaches zero and voltage V_{Cr} reaches its maximum value.

$$\theta = \omega_0 (t - t_2)$$

$$i_L(t) = i_L(t_2)\cos\theta - \frac{V_{Cr}(t_2)}{Z_0}\sin\theta \tag{5.14}$$

$$V_{Cr}(t) = V_{Cr}(t_2)\cos\theta + Z_0 i_L(t_2)\sin\theta \tag{5.15}$$

$$V_C(t) = 0 \tag{5.16}$$

$$i_L(t_3) = 0 \tag{5.17}$$

$$V_{Cr}(t_3) = \sqrt{\left(V_{Cr}(t_2)\right)^2 + \left(Z_0 i_L(t_2)\right)^2} \tag{5.18}$$

Mode M4 [t_3, t_4]**:** The current i_L remains at zero and cannot change its direction until the switch S_{r2} is turned on. The switch S_{r1} can be turned off at zero current. The duration of this mode is controllable and the switch S_{r2} can be turned on at any time. Now the total energy to bring the inverter input voltage to DC-link source voltage is stored in the resonant capacitor C_r. The voltage V_{Cr} is constant.

In case of topology T2, this energy is stored in resonant inductor L_r and the current i_L free wheels through the inverter switches and diode D_{r1}. The conduction losses occur in the inverter switches and diode D_{r1}, decreasing the efficiency of the total inverter.

$$i_L(t) = 0 \tag{5.19}$$

$$V_{Cr}(t) = V_{Cr}(t_3) \tag{5.20}$$

$$V_C(t) = 0 \tag{5.21}$$

Mode M5 [t_4, t_5]**:** To apply a new switching status to the inverter and to bring back the inverter voltage to DC-link voltage, the switch S_{r2} has to be turned on. A path for current i_L is built up and capacitor C_r starts discharging. The capacitor voltage V_{Cr} decreases and the inductor current i_L increases in a reverse direction.

$$\theta = \omega_0 (t - t_4)$$

$$i_L(t) = i_L(t_3)\cos\theta - \frac{V_{Cr}(t_3)}{Z_0}\sin\theta \tag{5.22}$$

$$V_{Cr}(t) = V_{Cr}(t_3)\cos\theta + Z_0 i_L(t_3)\sin\theta \tag{5.23}$$

$$V_C(t) = 0 \tag{5.24}$$

$$i_L(t_5) = I_{Tp2} \tag{5.25}$$

Mode M6 [t_5, t_6]**:** When the inductor current i_L is equal to second trip current I_{Tp2}, switch S_{INV} is turned off under zero voltage condition, i.e. a new switching status is applied to the inverter. The capacitor voltage V_{Cr} falls to zero as a result of resonance between C, C_r and L_r. At this point, diode D_r becomes forward biased and starts conducting, which avoids charging of the resonant capacitor in the reverse direction.

$$\theta = \omega_1 (t - t_5)$$

$$i_L(t) = \left(aI_O + i_L(t_5)\right)\cos\theta - \frac{V_{Cr}(t_5)}{Z_2}\sin\theta - aI_{OX} \tag{5.26}$$

$$V_{Cr}(t) = bV_{Cr}(t_5)\cos\theta + Z_3\left(aI_O + i_L(t_5)\right)\sin\theta + aV_{Cr}(t_5) - \frac{I_{OX}(t-t_5)}{C_{sum}} \tag{5.27}$$

$$V_C(t) = aV_{Cr}(t_5)(1-\cos\theta) - Z_1\left(aI_{OX} + i_L(t_5)\right)\sin\theta - \frac{I_{OX}(t-t_5)}{C_{sum}} \tag{5.28}$$

$$\text{At } t = t_6, V_{Cr}(t_6) = 0 \Rightarrow V_C(t_6) = \frac{Z_2}{Z_3}\left(a\,V_{Cr}(t_5) - \frac{I_{OX}(t-t_5)}{C_{sum}}\right) \tag{5.29}$$

$$i_L(t_6) = \sqrt{\left(aI_{OX} + i_L(t_5)\right)^2 + \left(\frac{V_{Cr}(t_5)}{Z_2}\right)^2 - \left(\frac{V_C(t_6)}{Z_2}\right)^2} - aI_{OX} \tag{5.30}$$

Mode M7 [t_6, t_7]**:** Due to resonance between C and L_r, the inverter voltage V_C reaches the DC-link source voltage V_{dc}. Then the switch S_{DC1} can be turned on under zero voltage condition.

$$\theta = \omega_2(t - t_6)$$

$$i_L(t) = \left(i_L(t_6) + I_{OX}\right)\cos\theta + \frac{V_C(t_6)}{Z_5}\sin\theta - I_{OX} \tag{5.31}$$

$$V_{Cr}(t) = 0 \tag{5.32}$$

$$V_C(t) = V_C(t_6)\cos\theta - Z_5\left(I_{OX} + i_L(t_6)\right)\sin\theta \tag{5.33}$$

$$\text{At } t = t_7, V_C(t_7) = V_{dc} \Rightarrow i_L(t_7) = -\sqrt{\left(I_{OX} + i_L(t_6)\right)^2 + \left(\frac{V_C(t_6)}{Z_5}\right)^2 - \left(\frac{V_{dc}}{Z_5}\right)^2} - I_{OX} \tag{5.34}$$

Mode M8 [t_8, t_9]**:** In this mode, the remaining energy stored in the inductor is fed back to the DC-link. The inductor current i_L goes back to zero from a negative value.

$$i_L(t) = i_L(t_8) + \frac{V_{dc}}{L_r}(t - t_8) \tag{5.35}$$

$$V_{Cr}(t) = 0 \tag{5.36}$$

$$V_C(t) = V_{dc} \tag{5.37}$$

5.2.1 Calculation of the Trip currents

In order to successfully control the inverter, the relation between trip currents (I_{Tp1} and I_{Tp2}) and inverter bridge input currents (I_O and I_{OX}) should be calculated. The calculation of the optimal trip currents is important in order to reduce the stress on the semiconductor devices and passive elements. The equations from (5.1) to (5.37) need to be solved for trip currents. The proposed QRDCL has 8 modes as shown in Figure 5.4 for

one resonant cycle. Because of 8 modes and 3 passive elements, an analytical solution turned out to be either impossible or at least highly complicated. The resonant circuit of topology T3 operates in a similar fashion as of topology T2, except during zero voltage period. So for the calculation of trip currents and design considerations, we can use an analogy between topology T2 and topology T3. The first two modes and last three modes are similar in both the topologies. For these modes, in both the topologies, all the state variables (i_L, V_{Cr} and V_C) are having the same initial and final values.

The trip currents for topology T2 are derived in section 2.3.1. If we observe the derivation, the zero voltage period equations are not used in calculating the trip currents. The trip currents indicate the energy stored in resonant inductor and capacitor. A sufficient energy should be stored to bring the inverter voltage return to DC-link voltage. During zero voltage period, this energy is stored in inductor L_r for topology T2 and in capacitor C_r for topology T3. For the calculation of trip currents, it is not important where the energy is stored. But it is important how much the energy need to be stored. So for the given resonant circuit elements and inverter input currents, the required trip currents are equal in both the topologies T2 and T3.

If the switch S_{r2} is closed forever, the topology T3 works in a similar way of topology T2. As a conclusion, the trip currents for topology T3 can be derived from topology T1 as discussed in section 2.3.1 and these trip currents are exactly equal to the values derived for topology T2.

5.2.2 Design Considerations

The converter is designed to achieve the voltage gradient of 600$V/\mu s$ intended for low over voltage at the end of a 34m motor cable. The design specifications are given in section 2.3.2. The voltage rising mode and falling mode are similar in both the topologies T2 and T3. The current i_L reaches its positive peak current during voltage falling mode. During the zero voltage period, resonant capacitor voltage reaches its peak value and remains at this value until the switch S_{r2} is turned on. This peak current and voltage are also same in both topologies. Ultimately, the design criterion is also same for both the topologies. The characteristics from Figure 2.12 to Figure 2.17 are also valid for topology T3. For the given specifications, the selected parameters are same and are as follows: Resonant Inductor L_r = 30µH, resonant capacitor C_r = 0.47 µF and capacitor C = 0.141 µF.

For the reduction of the common mode voltage level during zero voltage period, a complete separation of inverter and DC-link is possible with an additional switch S_{DC2}. In Figure 5.5, an added additional DC-link switch can be seen. The modulation scheme used is similar to the one discussed in section 2.4.1. As for the semiconductor devices, for DC-link switch, the CoolMOS selected in section 3.2.1 can be used. But for the resonant switches S_{r1} and S_{r2}, reverse blocking anti-parallel IGBTs are required.

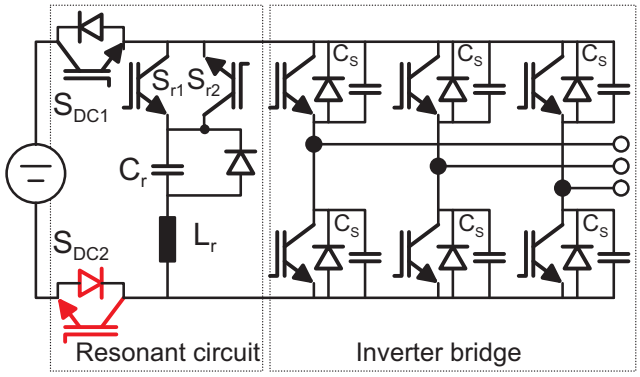


Figure 5.5 Modified circuit for CMV reduction

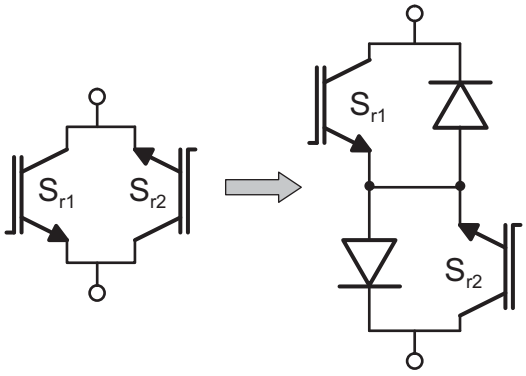


Figure 5.6 Equivalent switch

The discrete reverse blocking IGBTs (RB-IGBT) commercially available are from one company IXYS and can be connected in parallel. Results of the investigation in reference [78] point out that RB-IGBTs have superior conduction properties, but they suffer from unduly large reverse recover losses during switching. Using state of the art devices, the RB-IGBTs are an advantage at low switching frequencies and are not suitable in the place of resonant switches S_{r1} and S_{r2}. An equivalent circuit for antiparallel IGBTs is given in Figure 5.6. The reverse blocking IGBTs are not necessary for this representation. The selected 4th generation IGBTs from section 3.2.1 can be used. This structure increases losses due to additional 2 diodes, which carry the resonant current. However, for the current state of the art, the series connected IGBT-diode pairs have much smaller overall losses for the given application. If the reverse recovery characteristics of RB-IGBT are improved, it has an advantage of low power loss and smaller size compared to the series connected IGBT-diode pair. So the proposed resonant circuit will give good benefits with the future reverse blocking anti parallel IGBTs. The diode in parallel to the capacitance C_r should have a low reverse leakage current.

5.2.3 Control of the resonant converter

The control of the proposed resonant converter is similar to the resonant converter topology T2 except during the zero voltage period. The switching timings and the modified switching times are calculated as described in section 3.4.8 and section 3.4.9. From these timings, the switching instants are determined (section 3.4.10). Whenever a change in the switching status is needed, a 'Start' signal is generated. It initiates a resonant cycle. The state diagram for resonant circuit control is shown in Figure 5.7. The time (t_z) is equal to the modified zero vector time T_0^M.

The DC-link switches S_{DC1} and S_{DC2} are turned on and off at the same time. The resonant cycle is initiated with turn-on of the switch S_{r1}. When the required energy is stored in the resonant elements L_r and C_r, DC-link is separated from the inverter bridge. This moment is ascertained by comparing the inductor current with a trip current I_{Tp1}. When the inverter input voltage falls to zero, all the inverter switches are turned on. This instant is ensured by a zero voltage detection circuit. The zero voltage period of time is counted in FPGA and compared against required modified zero vector time. When the condition is satisfied, the switch S_{r2} is turned on and the switch S_{r1} is turned off.

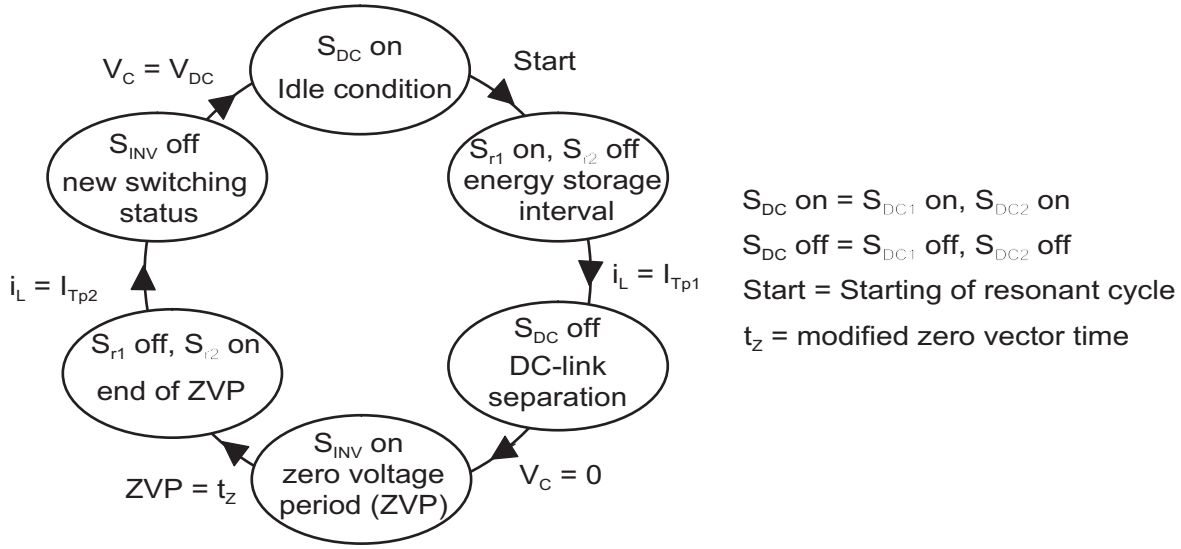


Figure 5.7 State diagram of proposed QRDCL inverter Control

When the inductor current reaches the second trip current level, the new switching status is applied to the inverter. Now the inverter input voltage rises to DC-link voltage and at this time, the DC-link switches are turned-on. The inverter input voltage's (V_C) zero voltage and full voltage detection can be done as discussed in section 3.2.3. Similarly, the inductor current against trip currents is compared as in section 3.2.3. When compared to topology T2, for this new proposed converter, any extra measurements are not necessary. At the end of a resonant cycle, remaining energy in the inductor is returned to the DC-link. The switch S_{r2} should be in on-state until i_L is zero. It can be switched off any time later. So the switch S_{r2} is turned off at the beginning of a resonant cycle.

5.2.4 Simulation of the resonant converter

To verify the proposed QRDCL inverter, zero voltage switching of the inverter and the lossless variable zero voltage duration, simulation with Simplorer® was accomplished. The resonant circuit parameters selected in section 5.2.2 are used in simulation. In Figure 5.8, simulated waveforms for resonant circuit are shown. In this case, the switch S_{r2} is closed with no delay. Then the resonant circuit works in similar fashion as of topology T2 and the waveforms are akin to the presented in Figure 2.18. The inverter bridge switches change their status when the inverter input voltage (V_C) is zero. For the designed resonant parameters, the peak capacitor voltage V_{Cr} is always less than the DC-link voltage. The resonant waveforms for extended resonant cycle are shown in Figure 5.9. During zero voltage period, the resonant capacitor voltage charged to its peak value and remained at this charge until the switch S_{r2} is turned on. At the same time, the inductor current i_L is zero. This zero voltage period is controllable and continues until the switch S_{r2} is turned on. Because the current i_L is zero, no current is freewheeling through the inverter devices. So a lossless variable zero voltage duration can be achieved by the proposed resonant converter. For given operating conditions, average value of the inductor current is less in topology T3 compared to topology T2.

Motor friendly characteristics like reduced output voltage gradients and reduced common mode voltages can also be achieved by the proposed resonant converter. The designed resonant circuit passive elements and load current decide the voltage gradient. Figure 5.10 shows the waveforms of a line to line voltage at the inverter and motor terminals for maximum load current. The overvoltage at motor terminals remains under 17% when using a 34m long cable. Here, the long cable simulation model is taken from [76]. The common mode voltage waveform is given in Figure 5.11. The common mode voltage level is reduced from $\pm V_{dc}/2$ to zero. The slope of the common mode voltage is also reduced.

To compare the two topologies T2 and T3, efficiency of both QRDCL inverters are determined through simulations. Reference [49], describes how to estimate power losses from simulation using ideal switches combined with measured power loss data and information from datasheets. For different speed and load torques, the input power, output power, output phase current and inductor losses are already measured experimentally for T2. In the simulation model of topology T3, the same inductor losses are maintained for given input conditions. The semiconductor devices conduction losses are taken from data sheets. The turn-on and turn-off energy losses provided in data sheets are for hard switching condition. All inverter bridge switches and DC-link switches (S_{DC1} and S_{DC2}) are turned off under ZVS but not under ZCS condition. For soft switching condition, i.e. ZVS turn-off or ZCS turn-on, the switching losses are taken such that the overall simulated losses equal to the experimentally measured losses. After calculating the loss parameters for a simulation model of topology T2, the same parameters are taken for a simulation model of topology T3.

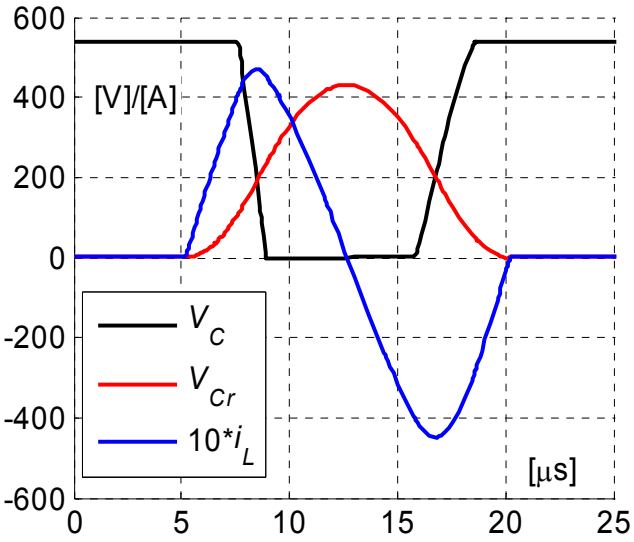


Figure 5.8 Simulated resonant circuit waveforms

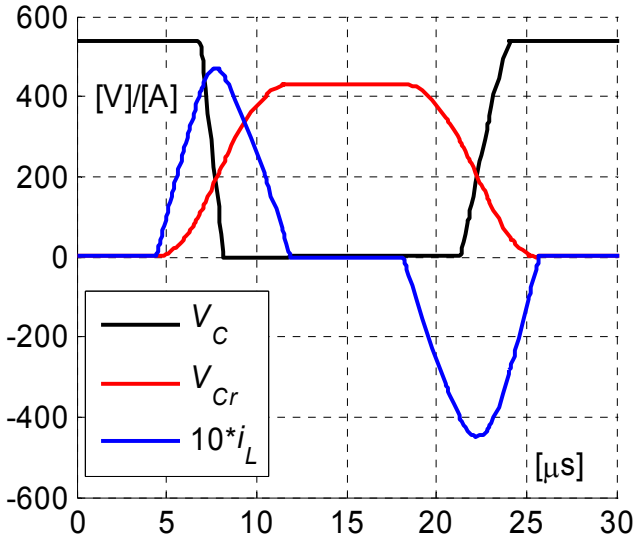


Figure 5.9 Simulated waveforms for extended zero voltage period

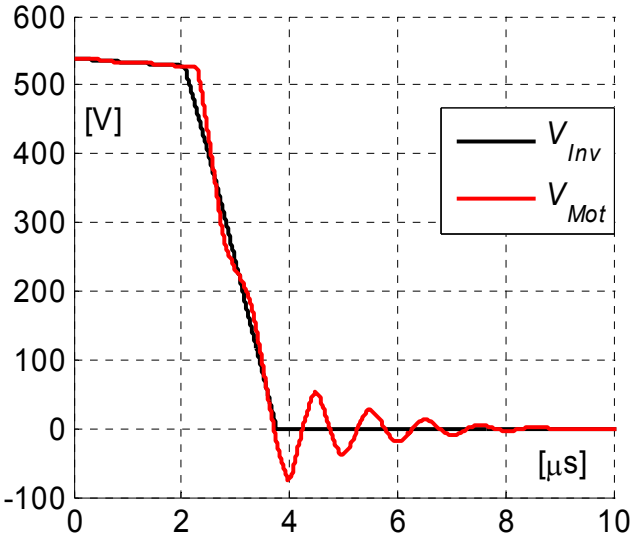


Figure 5.10 Simulated over voltage reflections

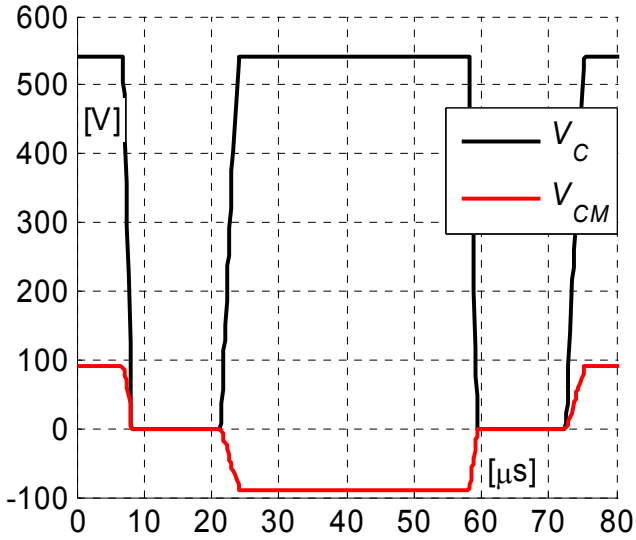


Figure 5.11 Simulated common mode voltage

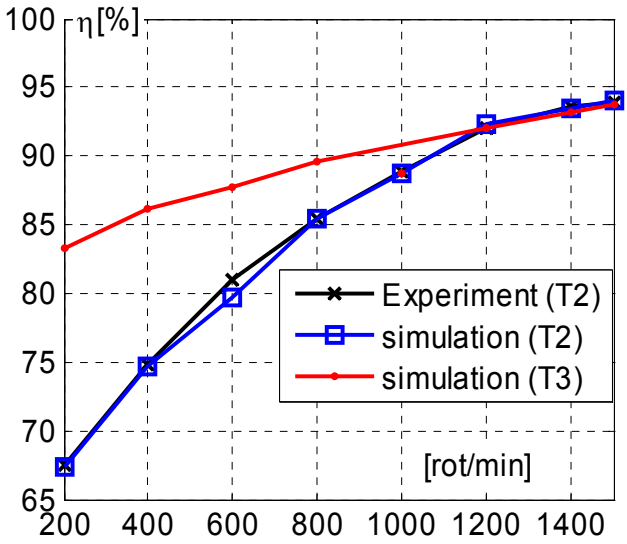


Figure 5.12 Efficiency plot (Torque = 10 Nm)

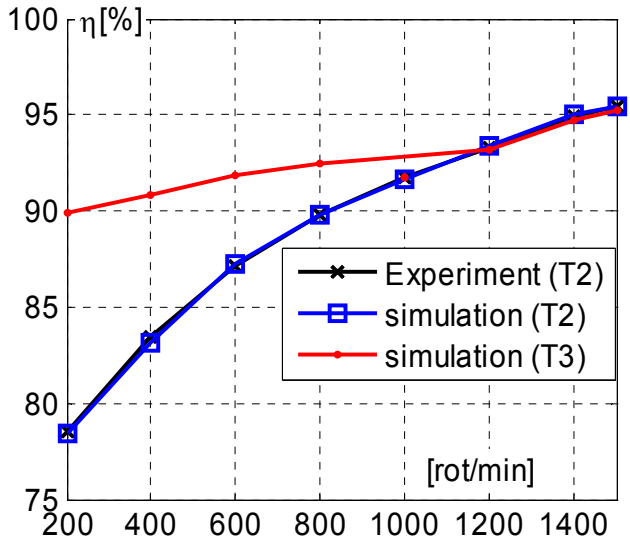


Figure 5.13 Efficiency plot (Torque = 20 Nm)

The efficiency is estimated for both the topologies and the efficiency plots are shown in Figure 5.12 and Figure 5.13. At low speeds, the efficiency of topology T3 is higher compare to topology T2. This can be attributed to the reduction of conduction losses during a resonant cycle's long zero voltage period. At higher speeds, the efficiency of topology T3 is same as topology T2. Here, a resonant cycle's zero voltage period is small and topology T3 works in a similar way of topology T2. So it can be concluded that the proposed QRDCL inverter helps in reducing the losses under the low modulation index.

5.3 Conclusions

The proposed QRDCL inverter is aimed at zero voltage switching and lossless variable zero voltage duration. The circuit operation principle is explained in detail. The mathematical equations for all the modes are also derived here. The design considerations and calculation of trip currents are similar to the topology T2. A control scheme of proposed resonant inverter is given. The QRDCL inverter is verified through the simulations. When the switch S_{r2} is closed, the circuit works in a similar way to the topology T2. So it can be concluded that the inverter works under real conditions. The lossless variable zero voltage duration is observed from simulations. The improved efficiency is also evaluated through simulation.

6 Conclusions

In this thesis, quasi-resonant DC link inverters for motor friendly application are investigated. The main results of a motor-friendly QRDCL inverter are summarized, and the future work is presented in this chapter.

6.1 Summary

Two quasi-resonant DC link inverters are designed, simulated and then compared. Finally, one quasi-resonant DC link inverter is selected and implemented for the reduction of high frequency parasitic effects. In chapter 2, the design expressions regarding the passive components selection are derived to meet certain criteria. The specific criteria selected for the design expressions is the maximum voltage derivative, low over voltage and current stress on the switching devices. However, the most important concern by the developed design is to guarantee the soft switching operation even under worst load conditions. A new modulation strategy is explained for a reduction of common mode voltage and better utilization of the DC-link voltage. An additional switch is added to the existing QRDCL inverter in order to separate the DC-link completely from the inverter bridge. With the help of the modified modulation and extended resonant cycle, common mode voltage level is reduced from $\pm V_{dc}$ / 2 to zero, which further leads to the reduction of bearing currents. To complete a resonant cycle, the optimum amount of energy needed to be stored in the resonant elements is calculated for all load conditions. It helps in reducing the losses and thereby to improve the efficiency of a quasi-resonant inverter. At the end, losses in the semiconductor devices are calculated based on the datasheet information.

The selection of the semiconductor devices is important in achieving high performance and low losses. In chapter 3, the power device selection consideration is discussed and is significant for the efficiency of an entire converter. The hardware and firmware developed for the control of QRDCL inverter is presented. The entire control of the inverter together with the induction motor is implemented in a FPGA. It reduces the total hardware count and provides a low cost solution.

The selected QRDCL inverter is built for a 4 kW nominal power. In chapter 4, the resonant link waveforms are shown and discussed. The reduction of high frequency parasitic effects is tested. The losses and efficiency of the entire QRDCL inverter are measured. The efficiency of a hard switching inverter with and without filters is also measured for comparison. Table 6.1 gives a comparative overview of the evaluated motor-friendly hard and soft switching inverters. The QRDCL inverter operating only for *dv/dt* reduction has higher efficiency compare to the HS inverter with a *dv/dt* filter. However, the efficiency of QRDCL inverter operating for *dv/dt* and CM voltage reduction is less than the HS inverter with a sine wave EMC filter. The reason for this is the losses during variable zero voltage duration of a resonant cycle.

In chapter 5, a novel QRDCL inverter is proposed and investigated. The proposed QRDCL inverter is aimed at reducing the high frequency parasitic effects and also provides loss less variable zero voltage duration. The mathematical analysis was carried out to determine the circuit operating equations. The design and control of the inverter are also given. The selection of the semiconductor devices is explained. The performance of this QRDCL inverter is verified through the simulations.

Table 6.1: Motor-friendly hard and soft switching inverters

Hard switching inverter with *dv/dt* output filter	**Soft switching inverter for *dv/dt* reduction**	**Hard switching inverter with sine - wave EMC output filter**	**Soft switching inverter for *dv/dt* and CM voltage reduction**
Advantages (+) / Disadvantages (–)			
+ No modification in the HS inverter control – increase in cost, size and weight – Lower efficiency	+ Small size and cost effective + Higher efficiency – Addition of the resonant circuit control	+ Sinusoidal output voltage and line to earth voltage + Higher efficiency – Expensive, heavy and bulky – Additional sensors for a short circuit detection – Filter time constant to be taken in the HS inverter control. Reduction in the control dynamic.	+ No output filters are required. Good dynamic characteristic. + Small size and cost effective + High efficiency is possible with loss less variable zero voltage period – Addition of the resonant circuit control and modified modulation – Low efficiency due to losses in the extended zero voltage period – Voltage-time error compensation is required
Application			
Over voltage reduction	Over voltage reduction	Over voltage, CM voltage reduction	Over voltage and CM voltage level reduction

6.2 Future work

By using latest developments in semiconductor technology available on the market, the efficiency can be further improved. In the future, when SiC FETs will be commercially available for e.g. 50A switches, then these devices will be highly interesting for this application. Use of the better inductor core will also improve the efficiency of SS inverter further. The proposed resonant circuit will give good benefits with the future reverse blocking anti parallel IGBTs.

In a hard switching inverter, rise time and fall time of output voltage is in nanoseconds. For a QRDCL inverter, these timings are designed to be longer to have reduced voltage gradients. The voltage error is the difference between reference voltage and output voltage. The volts-second error, which is the integral of the voltage error, is because of the slow rise and fall time of output voltage. The volts-second error compensation is required for a soft switching inverter as dead time compensation in a hard switching inverter. However, for given resonant elements, the rise and fall times are not constant but depend upon the load currents. The methods to minimize the volts-second error should be investigated.

Bibliography

[1] N. Mohan, *Electric drive: an integrative approach*. Minneapolis: MNPERE, 2001.

[2] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: converters, applications, and design*. 3rd ed. Hoboken, NJ: John Wiley & Sons, 2003.

[3] B. K. Bose, *Power electronics and variable frequency drives: technology and applications*. Piscataway, NJ: IEEE Press, 1996.

[4] P. Mutschler, "Advanced power electronics," Vorlesungsskript, Technische Universität Darmstadt, Darmstadt, 2007.

[5] V. Ramanarayanan, "Course material on switched mode power conversion," Department of Electrical Engineering, Indian Institute of Science, Bangalore, India, 2006.

[6] V. T. Ranganathan, "Course notes on electric drives," Department of Electrical Engineering, Indian Institute of Science, Bangalore, India, 2004.

[7] S. Round, M. Heldwein, J. Kolar, I. Hofsajer and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in *Proc.* 40th *Industry Applications Conference,* 2005, pp. 410-416.

[8] E. Persson, "Transient effects in application of PWM inverters to induction motors," *IEEE Transactions on Industry Applications,* vol. 28, pp. 1095-1101, 1992.

[9] S. Van Haute, A. Malfait, R. Reekmans and R. Belmans, "Losses, audible noise and overvoltages in induction motor drives," in 26th *Annual IEEE Power Electronics Specialists Conference,* 1995, pp. 586-592.

[10] L. A. Saunders, G. L. Skibinski, S. T. Evon and D. L. Kempkes, "Riding the reflected wave-IGBT drive technology demands new motor and cable considerations," in *Proc. IEEE Petroleum and Chemical Industry Conference*, 1996, pp. 75-84.

[11] G. Skibinski, J. Erdman, J. Pankau, and J. Campbell, "Assessing AC motor dielectric withstand capability to reflected voltage stress using corona testing," in *Proc. IEEE Industry Applications Conference*, 1996, pp. 694-702.

[12] A. Von Jouanne, P. Enjeti and W. Gray, "Application issues for PWM adjustable speed AC motor drives," *IEEE Industrial Applications Magazine*, vol. 2, Issue 5, pp. 10-18, Sep/Oct 1996.

[13] W. Santiago, "Inverter output filter effect on PWM motor drives of a flywheel energy storage system," in *Proc. Second International Energy Conversion Engineering Conference (NASA/TM-2004-213301)*, 2004.

[14] N. Hanigovszki, J. Landkildehus and F. Blaabjerg, "Output filters for AC adjustable speed drives," in *Proc. Applied Power Electronics Conference*, 2007, pp. 236-242.

[15] S. Melly, "New output filter concept for power drive systems," Schaffner EMC Inc., Internet: http://www.schaffner.com/mediapool/files/mediaPool49.pdf, Aug. 2002.

[16] "EMC filters," *Application notes*, EPCOS AG, 2006.

[17] "Output filters design guide," *Application notes*, Danfoss, 2010.

[18] "Proper grounding and VFD cables," *Application guide line #25,* Toshiba International Corporation.

[19] "3-line sine-wave EMC output filters B84143V*R127," *Datasheet*, EPCOS AG, Internet: www.epcos.com/inf/30/ds/b84143vr127.pdf, 2007.

[20] A. Muetze, "Bearing currents in inverter-fed AC motors," Ph.D. dissertation, Technische Universität Darmstadt, Darmstadt, 2004.

[21] A. V. Jouanne and G. L. Skibinski, "Design considerations for an inverter output filter to mitigate the effects of long motor leads in ASD applications," *IEEE Trans. on Industry Applications*, vol. 33, pp. 1138–1145, Sept/Oct. 1997.

[22] A. F. Moreira and T. A. Lipo, "Modeling and evaluation of *dv/dt* filters for AC drives with high switching speed," in *Proc. EPE*, CD-ROM, 2001.

[23] P. Feuerstack and B. Orlik, "EMC filter for PWM inverter fed motor drives to suppress traveling waves on long power lines between inverter and motor," in *Proc. EPE*, CD-ROM,1999.

[24] M. Cacciato, A. Consoli, G. Scarcella and A. Testa, "Reduction of common mode currents in PWM inverter motor drives," *IEEE Transactions on Industry Applications*, vol. 35, pp. 469-476, 1999.

[25] N. Aoki, K. Satoh, and A. Nabae, "Damping circuit to suppress motor terminal overvoltage and ringing in PWM inverter-fed AC motor drive systems with long motor leads," *IEEE Transactions on Industry Applications,* vol. 35, pp. 1014-1020, 1999.

[26] A.F. Moreira, T.A. Lipo, G. Venkataramanan, and S. Bernet, "High-frequency modeling for cable and induction motor overvoltage studies in long cable drives," *IEEE Transactions on Industry Applications,* vol. 38, pp. 1297-1306, 2002.

[27] G. Oriti, A.L. Julian and T.A. Lipo, "A new space vector modulation strategy for common mode voltage reduction," in *Proc. Power Electronics Specialists Conference*, 1997, pp. 1541-1546.

[28] H. D. Lee and S. K. Sul, "Common mode voltage reduction method modifying the distribution of zero voltage vector in PWM converter/inverter system," in *Proc. Industry Applications Conference,* 1999, pp. 1596-1601.

[29] D.M. Divan, "The Resonant DC Link Converter - A New Concept in Static Power Conversion," in *Proc. IEEE-IAS Conf. Rec.,* 1986, pp. 648-656.

[30] D.M. Divan and G. Skibinski, "Zero Switching Loss Inverters for High Power Applications," in *Proc. IEEE-IAS Conf. Rec*., 1987, pp. 627-634.

[31] D.M. Divan, L. Malesani, P. Tenti and V. Toigo, “A Synchronized Resonant DC Link Converter for Soft-Switched PWM,” *IEEE Trans. Industry Applications*, vol. 29, no. 5, pp. 940-948, Sept./Oct. 1993.

[32] S.G. Abeyratne, M.T. Aydemir, T.A. Lipo, Y. Murai and M. Yoshida, “Current Clamped, PWM, Quasi-Resonant, DC Link Series Resonant Converter,” in *Proc. IEEE-IAS Conf. Rec.*, 1994, pp. 820-826.

[33] V.G. Agelidis, P.D. Ziogas and G. Joos, “An Optimum Modulation Strategy for A Novel ”Notch” Commutated 3-F PWM Inverter,” *IEEE Trans. Industry Applications*, vol. 30, no. 1, pp. 52-61, Jan./Feb. 1994.

[34] A. Sikorski and T. Citko, “Quasi-Resonant Parallel DC Link Circuit for High-Frequency DC-AC Inverters,” in *Proc. EPE*, 1993, pp. 174-177.

[35] S. Chen and T.A. Lipo, “A Novel Soft-Switched PWM Inverter for AC Motor Drives,” *IEEE Trans. Power Electronics*, vol. 11, no. 4, pp. 653-659, July 1996.

[36] S. Salama and Y. Tadros, “Novel Soft Switching Quasi Resonant 3-Phase IGBT Inverter,” in *Proc. EPE*, Spain, 1995, pp. 95-99.

[37] M.C. Cavalcanti, E.R.C. da Silva, R.N.C. Alves, A.M.N. Lima, and C.B. Jacobina, “Reducing losses in three phase PWM pulsed dc link voltage-type inverter systems,” *IEEE Trans. Industry Applications*, vol. 38, no. 4, pp. 1114-1122, Jul./Aug. 2002.

[38] S. Mandrek, and P.J. Chrzan, “Quasi-resonant dc-link inverter with a reduced number of active elements,” *IEEE Trans. on Industrial Electronics*, vol. 54, No. 4, pp. 2088-2094, Aug. 2007.

[39] J. He and N. Mohan, “Parallel Resonant DC Link Circuit – A Novel Zero Switching Loss Topology with Minimum Voltage Stresses,” *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 687- 694, Oct. 1991.

[40] J. He, N. Mohan and B. Wold, “Zero voltage switching PWM inverter for high frequency DC-AC power conversion,” *IEEE Transactions on Industrial Applications*, vol. 29, pp. 959-968, Sep/Oct. 1993.

[41] J.G. Cho, H.S. Kim, and G.H. Cho, “Novel soft switching PWM converter using a new parallel resonant dc-link,” in *Proc. IEEE PESC,* 1991, pp. 241-247.

[42] L. Malesani, P. Tenti, P. Tomasin and V. Toigo, “High efficiency quasi-resonant DC link three-phase power inverter for full-range PWM,” *IEEE Transactions on Industry Applications*, vol. 31, pp. 141-148, Jan/Feb 1995.

[43] J.W. Choi and S.K. Sul, “Resonant link bidirectional power converter: Part I-Resonant circuit,” *IEEE Transactions on Power Electronics,* vol. 10, pp. 479-484, Jul 1995.

[44] J.S. Kim and S.K Sul, “Resonant link bidirectional power converter: Part II-Application to bidirectional AC motor drive without electrolytic capacitor,” *IEEE Transactions on Power Electronics,* vol. 10, pp. 485-493, Jul 1995.

[45] P. Karlsson, "*Quasi resonant DC link converters: analysis and design for a battery charger application*," Ph.D. dissertation, Dept. of Industrial Electrical Engineering and Automation, Lund Institute of Technology (Institutionen för industriell elektroteknik och automation, Lunds tekniska högsk.) (IEA), Lund, 1999.

[46] G. Bachmann and P. Mutschler, "Comparison of soft switched IGBT converters," in *Proc. Power conversion and intelligent motion conference (PCIM)*, 1999, pp. 469-474.

[47] G. Bachmann and P. Mutschler, "Comparison of PWM operated resonant DC voltage link inverters," in *Proc. European Conference on Power Electronics and Applications (EPE)*, 1999, pp. 1-3.

[48] Y.C. Jung, H.L. Liu, G.C. Cho and G.H. Cho, "Soft switching space vector PWM inverter using a new quasi-parallel resonant DC-link," *IEEE Transactions on Power Electronics*, vol. 11, pp. 503-510, May 1996.

[49] S. Munk-Nielsen, L.N. Tutelea and U. Jaeger, "Simulation with ideal switch models combined with measured loss data provides a good estimate of power loss," in *Proc. IEEE Industry Applications Conference,* 2000, pp. 2915-2922.

[50] L. Lorenz, G. Deboy, A. Knapp and M. Marz, "COOLMOS - a new milestone in high voltage power MOS," in *Proc. International Symposium on Power Semiconductor Devices and ICs*, 1999, pp. 3-10.

[51] S. Buonomo, C. Ronsisvalle, R. Scollo, S. Musumeci, R. Pagano and A. Raciti, "A new monolithic emitter-switching bipolar transistor (ESBT) in high-voltage converter applications," in *Proc. IEEE Industry Applications Society Annual Meeting,* 2003, pp. 1810-1817.

[52] S. Buonomo, V. Crisafulli, M. Nania, A. Raciti, C. Ronsisvalle and R. Scollo, "ESBT: power switch in high-power high-voltage converters," in *Proc. EPE*, 2007, pp. 1-10.

[53] V. Enea, D. Kroell, M. Messina and C. Ronsisvalle, "The ESBT (Emitter-Switched Bipolar Transistor): a new monolithic power actuator technology devoted to high voltage and high frequency applications," in *Proc. European Solid State Device Research Conference (ESSDERC)*, 2007, pp. 418-421.

[54] V. Enea, D. Kroell, M. Messina and C. Ronsisvalle, "Different designs for the optimization of monolithic ESBT(Emitter-Switched Bipolar Transistor)," in *Proc. International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2006, pp. 271-274.

[55] "Zero voltage switching and emitter switched bipolar transistor in a 3-phase auxiliary power supply," Application Note No. 2252, Internet: www.st.com/stonline/, Nov. 2006.

[56] A. Volke, M. Baessler, F. Umbach, F. Hille, W. Rusche and M. Hornkamp, "The new power semiconductor generation: 1200V IGBT4 and EmCon4 Diode," in Proc. of *India International Conference on power electronics*, pp. 77-82, 2006.

[57] P. Mutschler, "Control of Drives," Vorlesungsskript, Technische Universität Darmstadt, Darmstadt, 2007.

[58] D. Schröder, “Elektrische Antriebe 2,” Springer-Verlag Berlin Heidelberg New York, 1995.

[59] P. Mutschler, “Encoder Signal Processing”, *Instructions for practical training S*4, Technische Universität Darmstadt, Darmstadt, 2004.

[60] A. Glen Young, “How to use FPGAs for quadrature encoder-based motor control applications”, *Design Article,* Internet: www.eetimes.com, Nov. 2007.

[61] S. Senini and P. Wolfs, “Space Vector Modulation - A Novel implementation using Integer Microcontrollers,” in *Proc. AUPEC,* 2000, pp. 69-74.

[62] N. Janßen, “Aufbau eines Leistungsteils für resonant geschaltete Spannungszwischenkreis-Umrichter,” Diploma Thesis No. 1347, Technische Universität Darmstadt, Darmstadt, 2009.

[63] M. Krogemann and J. C. Clare, “A soft switching parallel quasi resonant DC-link inverter with modified asynchronous space vector PWM,” in *Proc. 6th International Conference on Power Electronics and Variable Speed Drives*, 1996, pp. 208-213.

[64] C. W. T. McLyman, *Transformer and inductor design handbook*. New York: Marcel Dekker, 2004.

[65] “Soft ferrites and accessories,” Ferroxcube data handbook, 2009.

[66] Y.Y. Tzau and H.J. Hsu, “FPGA realization of space vector PWM control IC for three phase PWM inverters,” *IEEE Transactions on Power Electronics,* vol. 12, pp. 953-963, Nov. 1997.

[67] K. De Brabandere, J. Van den Keybus, B. Bolsens, J. Driesen and R. Belmans, “FPGA-based current control of PWM voltage source inverters,” in *Proc. EPE,* 2003, pp. 1-10.

[68] R. Wu, D. Chen and S. Xie, “A three dimensional space vector modulation algorithm in A-B-C coordinate implemented by a FPGA,” in *Proc. IECON*, 2005, pp. 1071-1075.

[69] E. Monmasson and M.N. Cirstea, “FPGA design methodology for industrial control systems – A review,” *IEEE Transactions on Industrial Electronics*, vol. 54, pp.1824-1842, Aug. 2007.

[70] “Cyclone III device handbook, Volume 1,” Internet: www.altera.com, July 2008.

[71] “Cyclone III FPGA Starter board reference manual,” Internet: www.altera.com, April 2007.

[72] “Cyclone III FPGA Starter kit user guide,” Internet: www.altera.com, April 2007.

[73] R. De Doncker, “Zero voltage crossing detector for Soft switching devices,” U. S. Patent 5166549, November 24, 1992.

[74] R. Benavides Oswald, “Investigation of Control Methods for Segmented Long Stator Linear Drives,” Ph.D. dissertation, Technische Universität Darmstadt, Darmstadt, 2008.

[75] M. Mihalachi, “Position Acquisition and Control for Linear Direct Drives with Passive Vehicles,” Ph.D. dissertation, Technische Universität Darmstadt, Darmstadt, 2010.

[76] C. Purcarea, “High frequency parasitic effects in electric drives with long cables,” Ph.D. dissertation, Technische Universität Darmstadt, Darmstadt, 2011.

[77] K.A. Kwon, K.H. Kim, Y.C. Jung and M. Park, “New low loss quasi-parallel resonant DC-link inverter with lossless variable zero voltage duration,” in *Proc. 23rd International conference on Industrial Electronics, Control and Instrumentation (IECON)*, 1997, pp. 459-464.

[78] F. Kieferndorf, M. Forster, G. Venkataramanan and T.A. Lipo, “Current stiff rectifiers with reverse blocking IGBTs and IGBTs with series diodes,” *EPE 2003*, Toulouse, France, September 2-4, 2003.

Author’s Publications

[79] J. Kedarisetti and P. Mutschler, “A motor friendly quasi-resonant DC-link inverter with lossless variable zero voltage duration,” *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2613- 2622, May. 2012.

[80] J. Kedarisetti and P. Mutschler, “Control of a quasi-resonant DC-link soft switching inverter,” in *Proc. IEEE International Symposium on Industrial Electronics ISIE*, 2011, pp.171-176.

[81] J. Kedarisetti and P. Mutschler, “FPGA based control of quasi-resonant DC-link inverter and induction motor drive,” in *Proc. IEEE International Symposium on Industrial Electronics ISIE*, 2011, pp.1569-1574.

[82] J. Kedarisetti and P. Mutschler, “Efficiency comparison between motor friendly hard and soft switching inverters,” in *Proc. 14th European Conference on Power Electronics and Applications (EPE)*, 2011, pp. 1-10.

[83] J. Kedarisetti, C. Purcarea and P. Mutschler, “Design of a Quasi resonant DC-link soft switching inverter,” in *Proc. International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM)*, 2010, pp. 454-459.

[84] C. Purcarea, J. Kedarisetti and P. Mutschler, “A Motor Friendly and Efficient Resonant DC-link Converter,” in *Proc. 13th European Conference on Power Electronics and Applications (EPE)*, 2009, pp. 1-10.

Appendix

A. Inductor

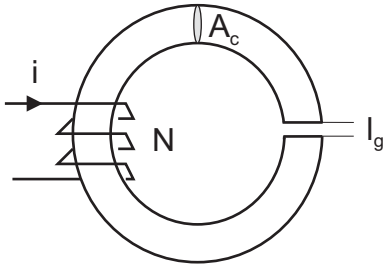


Figure A.1 A gapped iron core

For a gapped iron core, Ampere's circuit law gives:

$$N.i = H_c l_c + H_g l_g \tag{A.1}$$

Here, N denotes the number of winding turns. H_c and H_g are the magnetic field intensities in the core and air gap respectively. The magnetic flux mean path length in the core is l_c and in the air gap is l_g.

The magnetic flux densities B_c and B_g are defined as

$$B_c = \mu_0 \mu_r H_c \tag{A.2}$$

$$B_g = \mu_0 H_g \tag{A.3}$$

Where μ_0 is the permeability of the air and μ_r is the relative permeability of an iron core. Substituting into (A.1) gives:

$$N.i = \frac{B_c}{\mu_0 \mu_r} l_c + \frac{B_g}{\mu_0} l_g \tag{A.4}$$

Assuming the uniform flux densities, flux linkages is given by

$$\Psi = NB_c A_c = NB_g A_g \tag{A.5}$$

Where A_c and A_g are cross sectional areas of the iron core and air gap respectively. Fringing flux in the vicinity of the air gap is neglected, which is equivalent to

$$B_c = B_g \text{ and } A_c = A_g \tag{A.6}$$

Substituting (A.5) and (A.6) in (A.4) results:

$$N.i = \frac{\Psi}{\mu_0 N A_c}\left(\frac{l_c}{\mu_r} + l_g\right) \tag{A.7}$$

The inductance L is defined as

$$L = \frac{d\Psi}{di} \tag{A.8}$$

For a linear region,

$$L = \frac{\Psi}{i} \tag{A.9}$$

where ψ is the flux linkage resulting from the current i. Then

$$L = \frac{\mu_0 N^2 A_c}{\left(\frac{l_c}{\mu_c} + l_g\right)} \tag{A.10}$$

In most of the cases, the magnetic material has higher relative permeability. So the total reluctance of the circuit depends more on the air gap than on the iron core. The approximated L is given by

$$L = \frac{\mu_0 N^2 A_c}{l_g} \tag{A.11}$$

A.1 Inductor Core Size Selection

The inductor consists of a magnetic circuit and electric circuit. The design requires [5]:

1) *The size of the electric wire should be large enough to carry the rated current safely.*
2) *The size and shape of the magnetic core to be used such that*
   a. *The peak magnetic flux is carried safely without saturation.*
   b. *The windings are safely accommodated in the core.*
3) *The number of turns of the electric circuit to obtain the desired inductance.*

Any given conducting material can only carry a certain maximum current per unit of cross section of the wire size. When this limit is exceeded, the wire will over heat from the heat generated (I^2R) and melt or deteriorate. The safe current density of the conducting material is denoted by J (A/m^2).

Any magnetic material can only carry a certain maximum flux density. When this limit is exceeded, the material saturates and the relative permeability drops substantially. The allowable maximum flux density for a magnetic material is denoted by B_m (T).

The required size of the wire is

$$a_{cu} = I_{rms} / J \tag{A.12}$$

The peak flux density carried by the inductor (B_m) on the account of peak current (I_{peak}) is

$$LI_{peak} = N\phi_{peak} = NA_c B_m \tag{A.13}$$

The winding window area is A_w. The windings are safely accommodated in the core. The copper fill factor is K_w. Then

$$k_w A_w = Na_{cu} = NI_{rms} / J \tag{A.14}$$

Cross multiplying (A.13) and (A.14), we get

$$LI_{peak} \frac{I_{rms}}{J} = k_w B_m A_c A_w \Rightarrow LI_{peak} I_{rms} = k_w J B_m A_c A_w \tag{A.15}$$

The above equation may be interpreted as a relationship between the energy handling capacity ($LI_{peak}I_{rms}$) of the inductor to the size of the core ($A_C A_W$), the material properties (B_m, J), and our manufacturing skill (k_{cu}).

Table A.1: Inductor Specification

Inductance (L_r)	30 µH
Peak current (I_{peak})	60 A
RMS current (I_{rms})	38 A
Frequency (f)	72.46 kHz (13.8 µs)
Winding utilization factor (k_{cu})	0.3 (Litz wire)
Ambient Temperature (T_a)	25°C
Maximum Temperature (T_s)	100°C

A.2 Inductor Design

The specifications for design of a resonant inductor are given in Table A.1. The design steps are found in [2]. The stored energy in the inductor is given by ($LI_{peak}I_{rms}$), which is equal to 0.0684. The core size is chosen based on the value calculated in (A.15). For a constant current density, the resistivity of the copper windings and so the winding loss increases with temperature. For a constant flux density, the core loss increases with increasing temperature. Hence to reduce the losses, the device temperature should be maintained minimum. The internal temperature and the surface temperature are assumed to be nearly the same. That means the power dissipation is uniformly distributed throughout the inductor. This results, power dissipation density in the windings ($P_{w,sp}$) equal to the power dissipation density in the core ($P_{core,sp}$). This yields the highest value of the right hand side product in equation (A.15) [2].

The surface temperature (T_s) is determined by how efficiently the heat is transferred from the surface of a device to the ambient (T_a).

$$T_s = R_{\theta sa} P_{sp} \left(V_c + V_w \right) + T_a \tag{A.16}$$

P_{sp} is the allowable specific power density, which can be dissipated in the core and the winding. V_c and V_w are the core volume and winding volume respectively. The thermal resistance $R_{\theta sa}$ (surface to ambient) is the result of two heat transfer processes, convection and radiation. The thermal resistance due to radiative heat transfer is

$$R_{\theta,rad} = \frac{T_s - T_a}{5.7 * 10^{-8} E S_a ((T_s + 100)^4 - (T_a + 100)^4)} \ ^\circ C/W \tag{A.17}$$

E is the emissivity of the surface and for dark objects equal to 0.9 [2]. S_a is the outer surface area. The thermal resistance due to convective heat transfer is

$$R_{\theta,conv} = \frac{1}{1.34 S_a} \left(\frac{d_{vert}}{T_s - T_a} \right)^{1/4} \ ^\circ C/W \tag{A.18}$$

d_{vert} is the vertical height of the body and S_a is the outer surface area. The surface to ambient thermal resistance is

$$R_{\theta sa} = \frac{R_{\theta,rad} R_{\theta,conv}}{R_{\theta,rad} + R_{\theta,conv}} \ ^\circ C/W \tag{A.19}$$

For a selected material E71/33/32-3F3 material, the properties are given in Table A.2.

Table A.2: E71/33/32 Core

a	22 mm
d	32 mm
effective core area, A_c	683 mm^2
surface area, S_a	0.0219 m^2
Window area, A_w	569.4 mm^2
Effective core volume, V_c	102000 mm^3
Volume of the winding, V_w	84750 mm^3
vertical height of the body, d_{vert}	0.077 m

From equation (A.17), $R_{\theta,rad}$ = 5.85 °C/W.
From equation (A.18), $R_{\theta,conv}$ = 6.09 °C/W.
From equation (A.19), $R_{\theta,sa}$ = 2.98 °C/W.
The allowable specific power density, P_{sp} can be estimated by using (A.16).

$P_{sp} = P_{core,sp} = P_{w,sp}$ = 134.57 kW/m^3.

The power $P_{cu,sp}$ dissipated per unit of copper volume in a copper winding is given by

$$P_{cu,sp} = 22 * 10^{-9} * J_{rms}^2 \quad W/m^3 \tag{A.20}$$

The total volume of the copper is given by $V_{cu} = k_{cu} V_w$, where V_w is the total winding volume. Using this result, the power $P_{w,sp}$ dissipated per unit of winding volume is given by

$$P_{w,sp} = 22 * 10^{-9} * k_{cu} * J_{rms}^2 \quad W/m^3 \tag{A.21}$$

The rated current density J_{rms} is

$$J_{rms} = \sqrt{\frac{P_{w,sp}}{22 * 10^{-9} * k_{cu}}} = 4.5 * 10^6 \, A/m^2 \tag{A.22}$$

For the ferrite material 3F3,

$$P_{core,sp} = 1.5 * 10^{-3} * (f * 10^{-3})^{1.3} * (B_{ac} * 10^3)^{2.5} \quad W/m^3 \tag{A.23}$$

Solving equation for the rated flux density B_{ac} is given by

$$B_{ac} = \left(\frac{P_{core,sp}}{1.5 * 10^{-3} * (f * 10^{-3})^{1.3}} \right)^{0.4} * 10^{-3} = 0.1636 \quad T \tag{A.24}$$

The right hand side product of the equation (A.15) is $k_{cu} J_{rms} B_{ac} A_w A_{core} = 0.0862$. This value is greater than 0.0619 (= $L_r I_{peak} I_{rms}$).
The required conductor area

$$A_{cu} = \frac{I_{rms}}{J_{rms}} = 8.41 \quad mm^2 \tag{A.25}$$

During winding of the inductor, using Litz wire reduces the eddy current losses. A litz wire with cross sectional area of 10 mm^2 is used. The number of turns,

$$N = \frac{A_w k_{cu}}{A_{cu}} \approx 17 \tag{A.26}$$

The maximum inductance

$$L_{\max} = \frac{NA_c B_{ac}}{I_{peak}} = 31.6 \ \ \mu H \tag{A.27}$$

The number of winding turns required is given by the equation (A.28).

$$N = \frac{LI_{peak} A_c}{B_{ac}} \approx 16 \tag{A.28}$$

From equation (A.11), the total air gap length is calculated.

$$l_g = \frac{\mu_0 N I_{peak}}{B_{ac}} = 7.4 \ mm \tag{A.29}$$

The available air gap length (l_g) from the data sheet is 5.28 mm. The inductance will be higher than expected due to fringing fields. According to [64], the fringing flux factor, k_{ff} is calculated as

$$k_{ff} = 1 + \frac{l_g}{\sqrt{A_c}} \log\left(\frac{2D}{l_g}\right) = 1.568 \tag{A.30}$$

The fringing flux factor is used to adjust the number of turns, to compensate the fringing flux produced in the vicinity of the air gap.

$$N = \sqrt{\frac{l_g L}{\mu_0 A_c k_{ff}}} = 11 \tag{A.31}$$

The reduced turn's ratio means the peak magnetic flux density is greater than calculated in equation (A.24). From (A.13),

$$B_{ac} = \frac{LI_{peak}}{A_c N} = 0.2396 \tag{A.32}$$

The iron core loss for this peak flux density is calculated from the equation (A.23).

$$P_{core} = 36 \ W \tag{A.33}$$

To calculate the copper losses the mean length per turn (MLT) is calculated.

$$MLT = 2F + 2C + 2(E - F) = 0.16 \ m \tag{A.34}$$

The total winding resistance in the inductor is calculated at winding temperature 100°C.

$$R_{cu} = \frac{\rho_{cu}.N.MLT}{A_{cu}} = 5.8 \ m\Omega \tag{A.35}$$

The copper loss is given by

$$P_{cu} = I_{rms}^2 R_{cu} = 7.23 \ W \tag{A.36}$$

The most intense losses appear when the flux is concentrated by a magnetic circuit with an air gap and some conductors are close to that air gap. Here, the air gap losses are

not calculated. By avoiding to wind in the middle, eddy current losses in the presence of an air gap can be reduced [64].

Table A.3: Core comparison

Size	$P = P_{core} + P_w$	$B_{ac,Peak}\ (T)$	*N*	*Air gap* (mm)
E65/32/27-3F3	56 W	0.3030	11	4.1
E71/33/32-3F3	44 W	0.2396	11	5.28
E80/38/20-3F3	45 W	0.2701	17	10.8

Table A.3 compares three different core sizes. Here, the air gap losses are not included. The ferrite material 3C90 has lower core losses than 3F3 [65]. The efficiencies of a SS inverter for core types E71/33/32-3C90, E71/33/32-3F3 and E65/32/27-3C90 are measured. The efficiency is little higher with E65/32/27-3C90 core. The measurements in chapter 4 are presented for this core.

B. Technical data - Power Analyzer NORMA 5000

16.2 Technical data NORMA 5000

General technical data

Compact system	With 1 to 6 phases
	Continuous averages
Interface	Compatible to D5255
Housing	Metal housing
Weight	approx. 7 kg
Dimensions (W,H,D)	447 mm, 150 mm (3HU), 315 mm
Display	5.7", 320 x 240 pixel; background illumination and contrast adjustable
Operation	Membrane keyboard, with cursor, function keys and direct functions
Mains connection	85 ... 264 V AC, 47.. 440Hz, DC 120 ... 370 V, approx. 40 VA Euro plug with switch
Measuring terminals	4 mm guard sockets, 2 each per input; or screw terminals external shunt connection via BNC socket

Ambient conditions

Operating temperature range	+5 ... +35 °C
Storage temperature range	−20 ... +50 °C
Climatic class	B2 (according to IEC 60654-1)
Relative humidity	max. 85 %, noncondensing

Specifications

Voltage

8 measuring range for U	0.3 – 1 – 3 – 10 – 30 – 100 – 300 – 1000 V
U_{peak}	2 x measuring range
Input impedance	2 Mohm // 20 pF
Common mode rejection	120 dB at 100 kHz

Current

6 measuring ranges for I direct (10A)	30 – 100 mA – 0.3 – 1 – 3 – 10 A
6 measuring ranges for I direct (20A)	60 – 200 mA – 0.6 – 2 – 6 – 20 A
I_{peak}	2 x measuring range
Input impedance with integrated shunts (10A)	
Ranges	30, 100 mA: 1 ohm
	0.3, 1 A: 0.1 ohm
	3, 10 A: 0.01 ohm
Input impedance with integrated shunts (20A)	
Ranges	60, 200 mA: 0.5 ohm
	0.6, 2 A: 0.05 ohm
	6, 20 A: 0.005 ohm
Measuring connection for shunt or probe	
BNC socket	100 kOhm // 30pF
Ranges	30 – 100mV – 0.3 – 1 – 3 – 10 V
Overload (bar)	max. 20 V_{eff}
Common mode rejection	120 dB at 100 kHz

Limit of error

Power phase	PP30	PP40	PP42	PP50	PP51	PP52
Limit of error	U	U	U	U	U	U
reading	0,15%	0,10%	0,10%	0,05%	0,05%	0,05%
range	0,15%	0,10%	0,10%	0,05%	0,05%	0,05%
Limit of error	I	I	I	I	I	I
reading	0,15%	0,10%	0,10%	0,05%	0,05%	0,05%
range	0,15%	0,10%	0,10%	0,05%	0,05%	0,05%

This data is valid for averages and the following reference conditions:

- Ambient temperature 23 +- 0.5 °C, frequency 50 Hz, heat-up time of minimum 1 hour and incoming measuring signal.

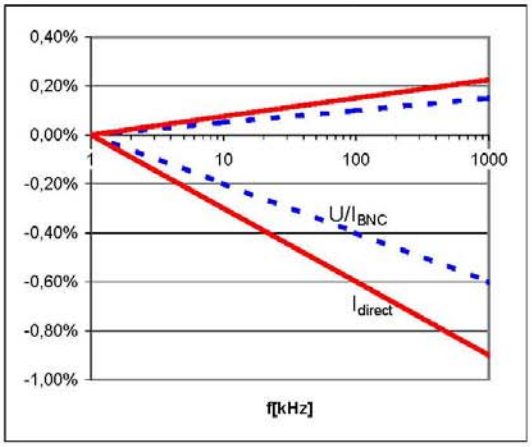
Sample rate

Power Phase	PP30	PP40	PP42	PP50	PP51	PP52	PP54
Sample rate	102kHz	341kHz	341kHz	1MHz	1MHz	341kHz	341kHz

Bandwidth

Bandwidth	U direct	I via BNC	I direct measured
PP30	1 MHz	1 MHz	0,3 MHz
PP40	3 MHz	3 MHz	1 MHz
PP42	3 MHz	3 MHz	0,5 MHz
PP50	10 MHz	10 MHz	1 MHz
PP51	3 MHz	3 MHz	1 MHz
PP52	3 MHz	3 MHz	0,5 MHz
PP54	3 MHz	3 MHz	1 MHz

Diagram Bandwidth (limit of error) Power Phase PP50:



Angle error

For accurate measurements, harmonics over 1 MHz may reach maximum half of the range.

Power phase PP30	between U and I_{BNC}	between U and I_{direct}
Angle error	0,1° + 0,1° /kHz	0,1° + 0,1° /kHz
All other power phases		
Angle error	0,005° + 0,005° /kHz	0,025° + 0,015° /kHz

Frequency and synchronisation

Range	0.2Hz ... Sample rate (102kHz / 341kHz / 1MHz)
Measurement error	±0.01% rdg
Channel selection	all channels U/I, or external input
Low-pass filter	optionally integratable, with 3 different limit frequencies
External Sync-input	Max. 50V, 0,2Hz to sample rate
Sync-output	Pulsed TTL signal 5V

Data memory

Measured data memory	approx. 4 MB

Configuration memory

The current instrument settings can be stored as configurations in a non-volatile memory for subsequent reloading. Changes that are not saved in a configuration are lost when the device is switched off. Up to 15 user-defined configurations can be permanently stored under predefined names.

Interfaces

RS 232	RS 232 interface for firmware upload and data exchange with PC; the device can be connected to a printer through an external adapter
GPIB	IEEE 488.2 / 1 MBit/s
LAN	Ethernet / 10 MBits/s or 100 MBits/s
USB	USB2.0

Standards

Electrical safety	
EN 61010-1/ 2. edition 1000V CAT II (600V CAT III)	Degree of pollution 2, Protection class I
EN 61558	for transformer
EN 61010-2-031/032	for accessories
Electromagnetic compatibility	
Emission	IEC 61326-1, EN 50081-1, EN 55011 class B
Immunity	IEC 61326-1 / annex A (industrial), EN 50082-1
Max. input voltage	
for voltage inputs	Range 1000 V_{eff}, 2 kV_{peak}
for current inputs	Range 10 A_{eff}, 20 A_{peak}
Test voltages	
Mains input housing (earth connector)	1.5 KV a.c.
Mains connection measuring inputs	5.4 kV a.c.
Measuring inputs housing	3.3 kV a.c.
Measuring input measuring input	5.4 kV

C. Datasheets

C.1 CoolMOS Power Transistor

IPW60R045CP

CoolMOS® Power Transistor

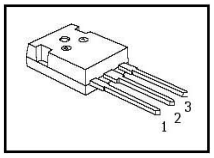
Features

- Worldwide best $R_{ds,on}$ in TO247
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant

Product Summary

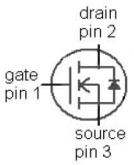
V_{DS} @ T_{jmax}	650	V
$R_{DS(on),max}$	0.045	Ω
$Q_{g,typ}$	150	nC

PG-TO247-3-1



CoolMOS CP is specially designed for:

- Hard switching SMPS topologies



Type	Package	Ordering Code	Marking
IPW60R045CP	PG-TO247-3-1	SP000067149	6R045

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	60	A
		T_C=100 °C	38	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	230	
Avalanche energy, single pulse	E_{AS}	I_D=11 A, V_{DD}=50 V	1950	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=11 A, V_{DD}=50 V	3	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		11	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...480 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	431	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	T_C=25 °C	44	A
Diode pulse current[2]	$I_{S,pulse}$		230	
Reverse diode dv/dt[4]	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.29	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=3 mA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C	-	-	10	µA
		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C	-	50	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=44 A, T_j=25 °C	-	0.04	0.045	Ω
		V_{GS}=10 V, I_D=44 A, T_j=150 °C	-	0.11	-	
Gate resistance	R_G	f=1 MHz, open drain	-	1.3	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	6800	-	pF
Output capacitance	C_{oss}		-	320	-	
Effective output capacitance, energy related[5)]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 480 V	-	310	-	
Effective output capacitance, time related[6)]	$C_{o(tr)}$		-	820	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=400 V, V_{GS}=10 V, I_D=44 A, R_G=3.3 Ω	-	30	-	ns
Rise time	t_r		-	20	-	
Turn-off delay time	$t_{d(off)}$		-	100	-	
Fall time	t_f		-	10	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=44 A, V_{GS}=0 to 10 V	-	34	-	nC
Gate to drain charge	Q_{gd}		-	51	-	
Gate charge total	Q_g		-	150	190	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=44 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=I_S, di_F/dt=100 A/µs	-	600	-	ns
Reverse recovery charge	Q_{rr}		-	17	-	µC
Peak reverse recovery current	I_{rrm}		-	60	-	A

[1)] J-STD20 and JESD22

[2)] Pulse width t_p limited by $T_{j,max}$

[3)] Repetitive avalanche causes additional power losses that can be calculated as P_{AV}=E_{AR}*f.

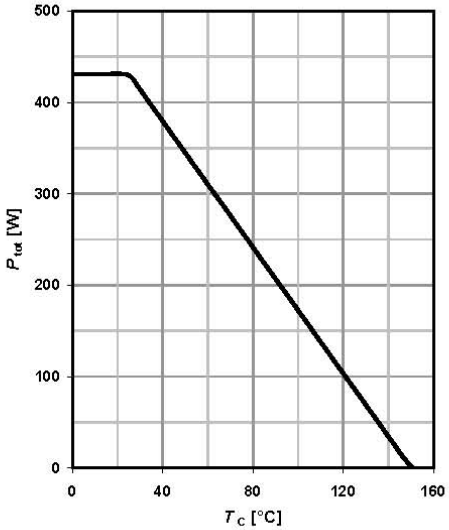
[4)] I_{SD}≤I_D, di/dt≤100A/µs,V_{DClink} = 400V, Vpeak<$V_{(BR)DSS}$, T_j<T_{jmax}, identical low side and high side switch

[5)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[6)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

1 Power dissipation

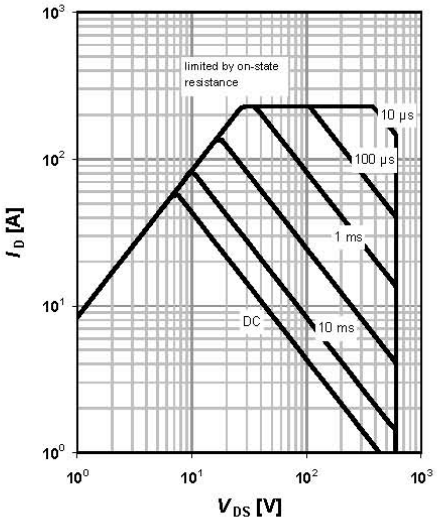
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

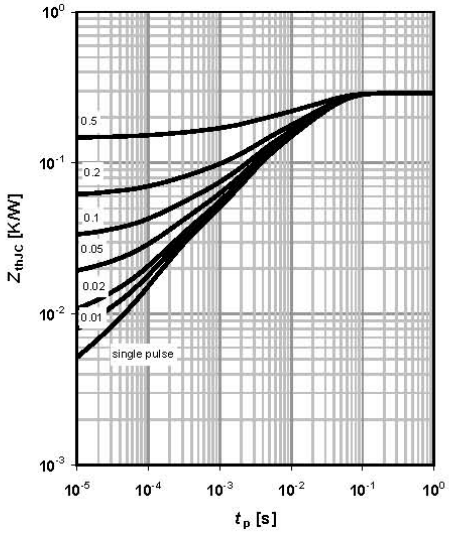
parameter: t_p



3 Max. transient thermal impedance

$Z_{(thJC)}=f(t_p)$

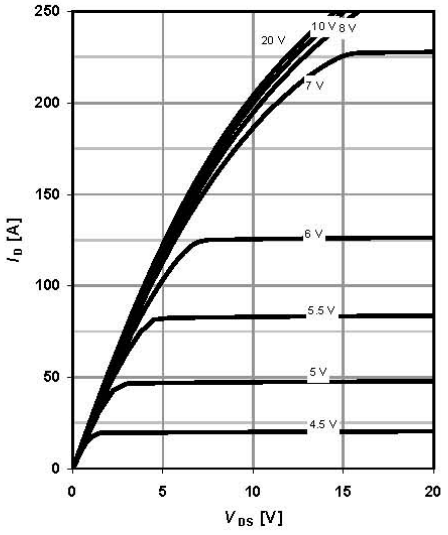
parameter: $D=t_p/T$



4 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

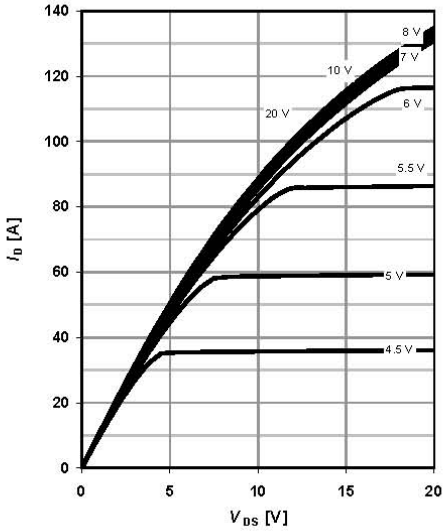
parameter: V_{GS}



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=150$ °C

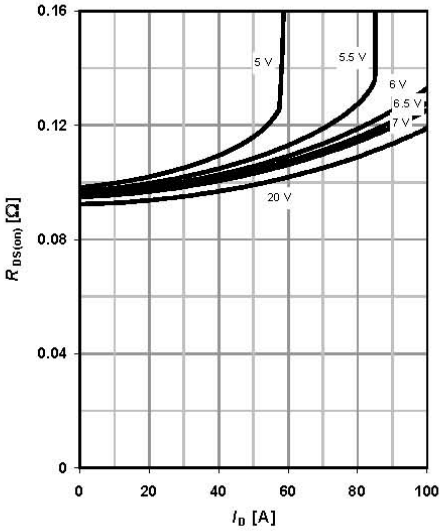
parameter: V_{GS}



6 Typ. drain-source on-state resistance

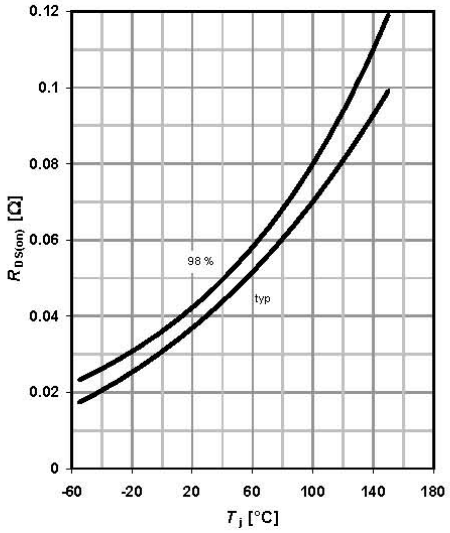
$R_{DS(on)}=f(I_D)$; $T_j=150$ °C

parameter: V_{GS}



7 Drain-source on-state resistance

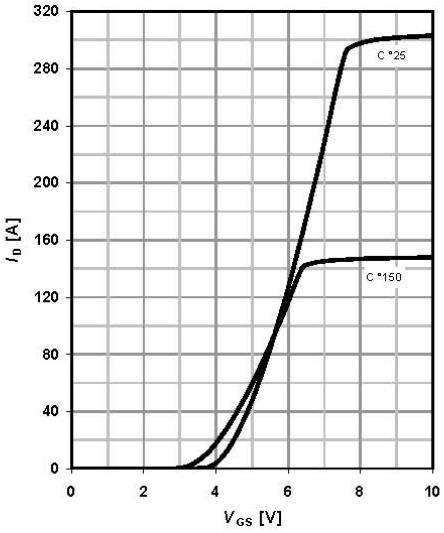
$R_{DS(on)}=f(T_j)$; $I_D=44$ A; $V_{GS}=10$ V



8 Typ. transfer characteristics

$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

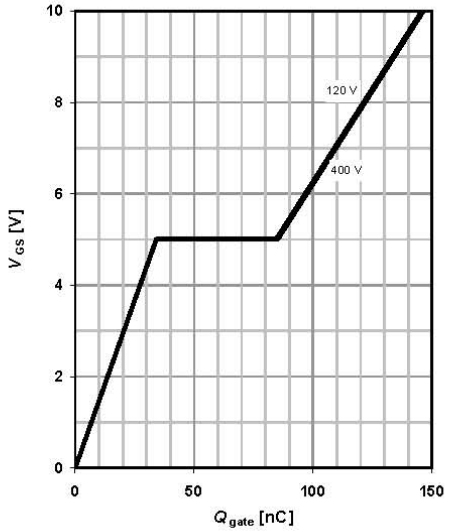
parameter: T_j



9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=44 A pulsed

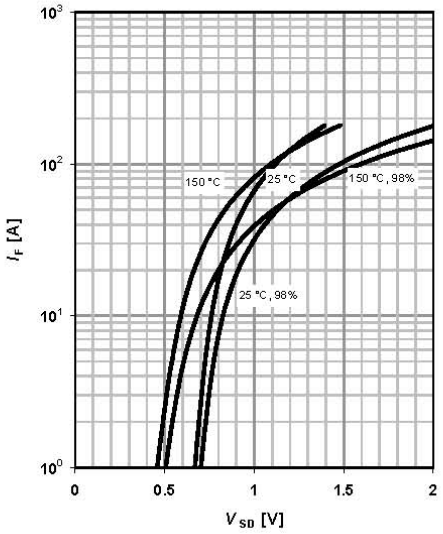
parameter: V_{DD}



10 Forward characteristics of reverse diode

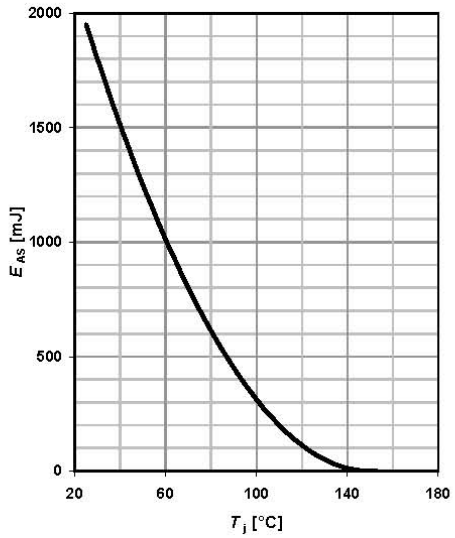
I_F=f(V_{SD})

parameter: T_j



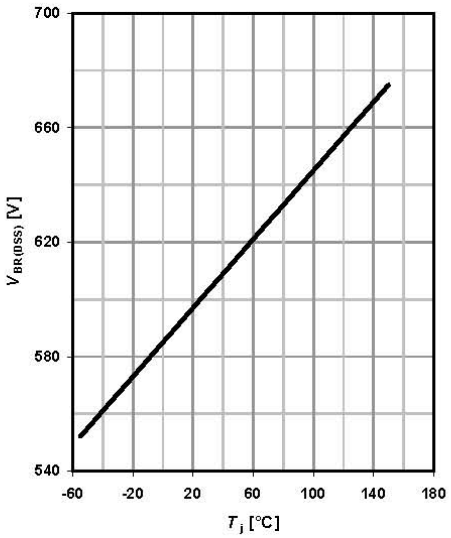
11 Avalanche energy

E_{AS}=f(T_j); I_D=11 A; V_{DD}=50 V



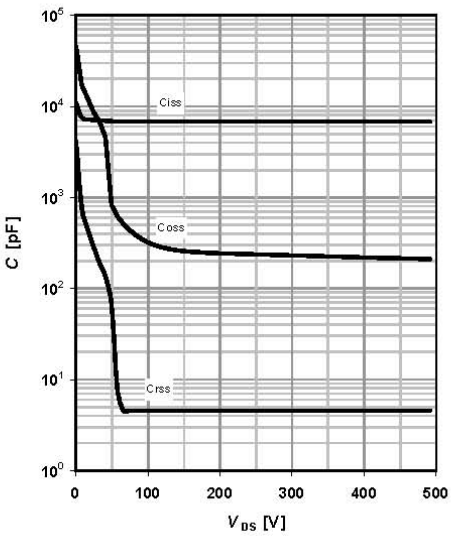
12 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA



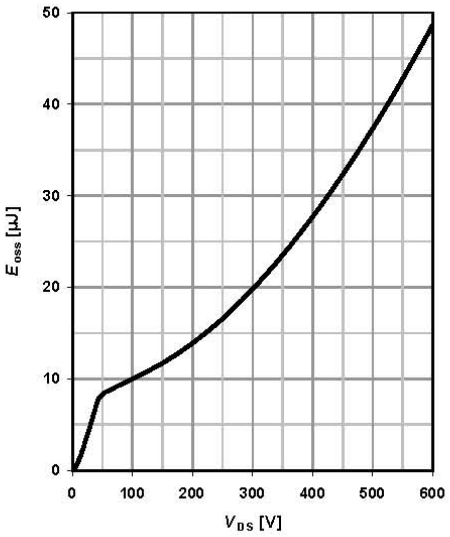
13 Typ. capacitances

$C = f(V_{DS})$; V_{GS}=0 V; f=1 MHz



14 Typ. Coss stored energy

$E_{oss} = f(V_{DS})$



C.2 IGBT Inverter Module

Technische Information / technical information

IGBT-Module
IGBT-modules

FS75R12KT4_B15

EconoPACK™2 Modul mit Trench/Feldstopp IGBT4 und Emitter Controlled4 Diode
EconoPACK™2 module with trench/fieldstop IGBT4 and Emitter Controlled4 Diode

IGBT-Wechselrichter / IGBT-inverter — Vorläufige Daten / preliminary data

Höchstzulässige Werte / maximum rated values

Kollektor-Emitter-Sperrspannung collector-emitter voltage	T_{vj} = 25°C	V_{CES}	1200		V
Kollektor-Dauergleichstrom DC-collector current	T_C = 95°C, T_{vj} = 175°C	$I_{C\,nom}$	75		A
Periodischer Kollektor Spitzenstrom repetitive peak collector current	t_P = 1 ms	I_{CRM}	150		A
Gesamt-Verlustleistung total power dissipation	T_C = 25°C, T_{vj} = 175°C	P_{tot}	385		W
Gate-Emitter-Spitzenspannung gate-emitter peak voltage		V_{GES}	+/-20		V

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Kollektor-Emitter Sättigungsspannung collector-emitter saturation voltage	I_C = 75 A, V_{GE} = 15 V, T_{vj} = 25°C I_C = 75 A, V_{GE} = 15 V, T_{vj} = 125°C I_C = 75 A, V_{GE} = 15 V, T_{vj} = 150°C	$V_{CE\,sat}$		1,85 2,15 2,25	2,15	V V V
Gate-Schwellenspannung gate threshold voltage	I_C = 2,40 mA, V_{CE} = V_{GE}, T_{vj} = 25°C	V_{GEth}	5,2	5,8	6,4	V
Gateladung gate charge	V_{GE} = -15 V ... +15 V	Q_G		0,57		µC
Interner Gatewiderstand internal gate resistor	T_{vj} = 25°C	R_{Gint}		10		Ω
Eingangskapazität input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V	C_{ies}		4,30		nF
Rückwirkungskapazität reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V	C_{res}		0,16		nF
Kollektor-Emitter Reststrom collector-emitter cut-off current	V_{CE} = 1200 V, V_{GE} = 0 V, T_{vj} = 25°C	I_{CES}			1,0	mA
Gate-Emitter Reststrom gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C	I_{GES}			100	nA
Einschaltverzögerungszeit (ind. Last) turn-on delay time (inductive load)	I_C = 75 A, V_{CE} = 600 V, V_{GE} = ±15 V, R_{Gon} = 2,2 Ω; T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,on}$		0,13 0,15 0,15		µs µs µs
Anstiegszeit (induktive Last) rise time (inductive load)	I_C = 75 A, V_{CE} = 600 V, V_{GE} = ±15 V, R_{Gon} = 2,2 Ω; T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r		0,02 0,03 0,035		µs µs µs
Abschaltverzögerungszeit (ind. Last) turn-off delay time (inductive load)	I_C = 75 A, V_{CE} = 600 V, V_{GE} = ±15 V, R_{Goff} = 2,2 Ω; T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,off}$		0,30 0,38 0,40		µs µs µs
Fallzeit (induktive Last) fall time (inductive load)	I_C = 75 A, V_{CE} = 600 V, V_{GE} = ±15 V, R_{Goff} = 2,2 Ω; T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_f		0,045 0,08 0,09		µs µs µs
Einschaltverlustenergie pro Puls turn-on energy loss per pulse	I_C = 75 A, V_{CE} = 600 V, L_S = 25 nH, V_{GE} = ±15 V, di/dt = 2800 A/µs (T_{vj}=150°C), R_{Gon} = 2,2 Ω; T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}		4,70 7,20 8,00		mJ mJ mJ
Abschaltverlustenergie pro Puls turn-off energy loss per pulse	I_C = 75 A, V_{CE} = 600 V, L_S = 25 nH, V_{GE} = ±15 V, du/dt = 3800 V/µs (T_{vj}=150°C), R_{Goff} = 2,2 Ω; T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}		3,90 6,10 6,40		mJ mJ mJ
Kurzschlussverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 800 V, V_{CEmax} = V_{CES} -L_{sCE} ·di/dt; t_P ≤ 10 µs, T_{vj} = 150°C	I_{SC}		270		A
Innerer Wärmewiderstand thermal resistance, junction to case	pro IGBT / per IGBT	R_{thJC}			0,39	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,195		K/W

prepared by: Christoph Messelke	date of publication: 2008-05-15
approved by: Robert Severin	revision: 2.0

1

Technische Information / technical information

IGBT-Module
IGBT-modules

FS75R12KT4_B15

Vorläufige Daten
preliminary data

Diode-Wechselrichter / diode-inverter

Höchstzulässige Werte / maximum rated values

Periodische Spitzensperrspannung repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	1200		V
Dauergleichstrom DC forward current		I_F	75		A
Periodischer Spitzenstrom repetitive peak forward current	t_P = 1 ms	I_{FRM}	150		A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	960		A²s

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Durchlassspannung forward voltage	I_F = 75 A, V_{GE} = 0 V I_F = 75 A, V_{GE} = 0 V I_F = 75 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	V_F		1,70 1,65 1,65	2,15	V V V
Rückstromspitze peak reverse recovery current	I_F = 75 A, - di_F/dt = 2800 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}		115 120 125		A A A
Sperrverzögerungsladung recovered charge	I_F = 75 A, - di_F/dt = 2800 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r		8,60 14,0 16,0		µC µC µC
Abschaltenergie pro Puls reverse recovery energy	I_F = 75 A, - di_F/dt = 2800 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}		2,60 4,50 5,50		mJ mJ mJ
Innerer Wärmewiderstand thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			0,62	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,31		K/W

NTC-Widerstand / NTC-thermistor

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Nennwiderstand rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R_{100} deviation of R_{100}	T_C = 100°C, R_{100} = 493 Ω	$\Delta R/R$	-5		5	%
Verlustleistung power dissipation	T_C = 25°C	P_{25}			20,0	mW
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/50}(1/T_2 - 1/(298,15\ K))]$	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/80}(1/T_2 - 1/(298,15\ K))]$	$B_{25/80}$		3411		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/100}(1/T_2 - 1/(298,15\ K))]$	$B_{25/100}$		3433		K

Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

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Technische Information / technical information

IGBT-Module
IGBT-modules

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Vorläufige Daten
preliminary data

Modul / module

Isolations-Prüfspannung insulation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		2,5		kV
Material Modulgrundplatte material of module baseplate				Cu		
Material für innere Isolation material for internal insulation				Al_2O_3		
Kriechstrecke creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			10,0		mm
Luftstrecke clearance distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			7,5		mm
Vergleichszahl der Kriechwegbildung comparative tracking index		CTI		> 200		
			min.	typ.	max.	
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,02		K/W
Modulinduktivität stray inductance module		L_{sCE}		19		nH
Modulleitungswiderstand, Anschlüsse - Chip module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		1,80		mΩ
Höchstzulässige Sperrschichttemperatur maximum junction temperature	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	$T_{vj\ max}$			175	°C
Temperatur im Schaltbetrieb temperature under switching conditions	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	$T_{vj\ op}$	-40		150	°C
Lagertemperatur storage temperature		T_{stg}	-40		125	°C
Anzugsdrehmoment f. mech. Befestigung mounting torque	Schraube M5 - Montage gem. gültiger Applikation Note screw M5 - mounting according to valid application note	M	3,00	-	6,00	Nm
Gewicht weight		G		180		g

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Vorläufige Daten
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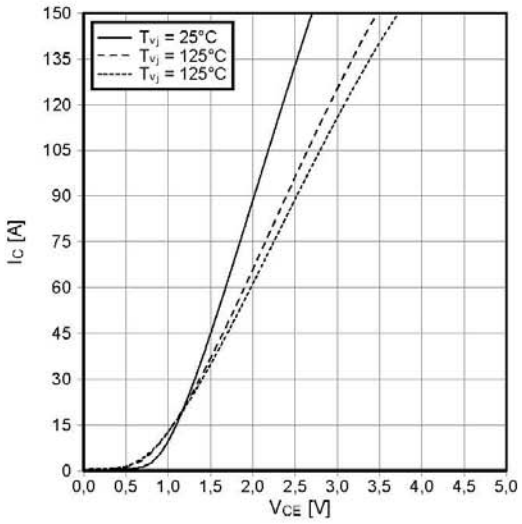
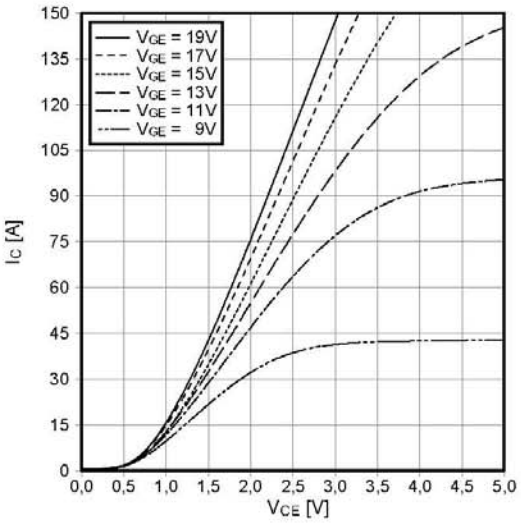
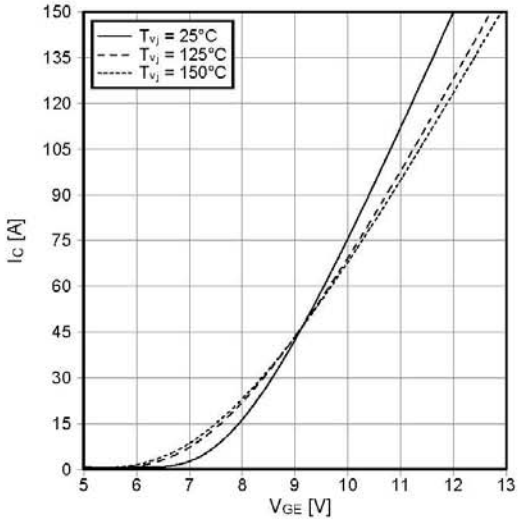
Ausgangskennlinie IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



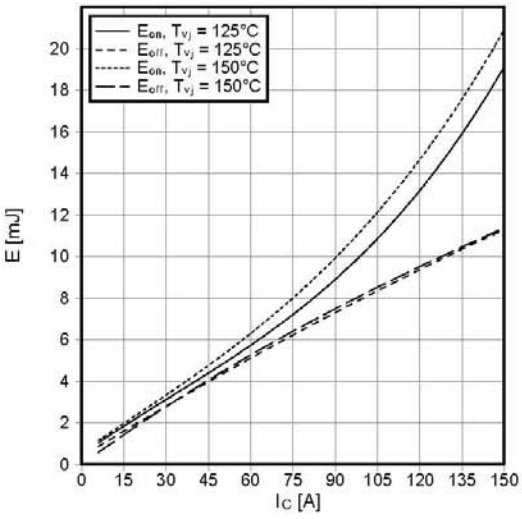
Ausgangskennlinienfeld IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 150°C



Übertragungscharakteristik IGBT-Wechselr. (typisch)
transfer characteristic IGBT-inverter (typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V



Schaltverluste IGBT-Wechselr. (typisch)
switching losses IGBT-inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 2.2 Ω, R_{Goff} = 2.2 Ω, V_{CE} = 600 V



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Technische Information / technical information

IGBT-Module
IGBT-modules

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Vorläufige Daten
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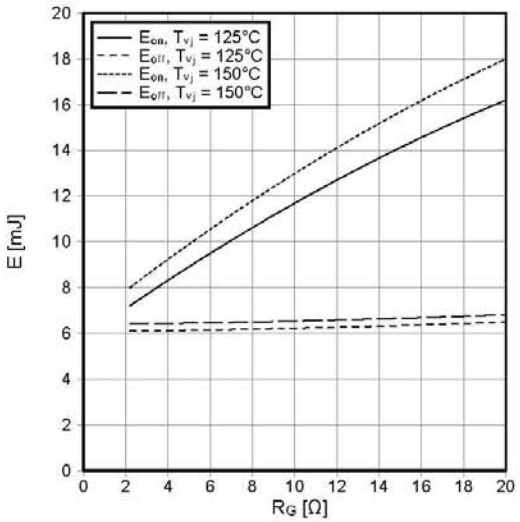
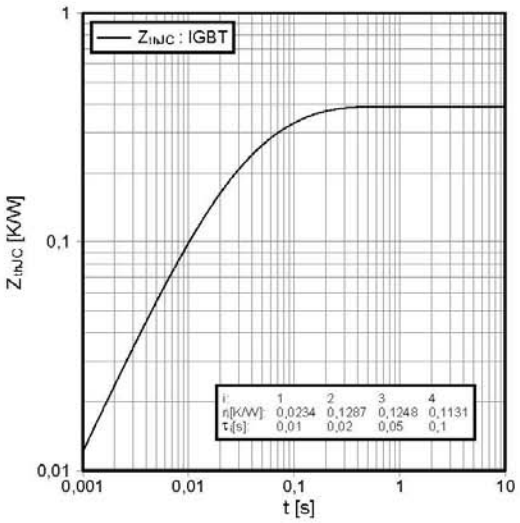
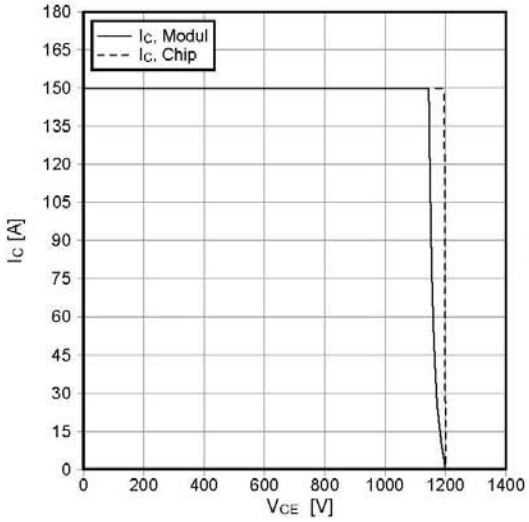
Schaltverluste IGBT-Wechselr. (typisch)
switching losses IGBT-Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
$V_{GE} = \pm 15$ V, $I_C = 75$ A, $V_{CE} = 600$ V



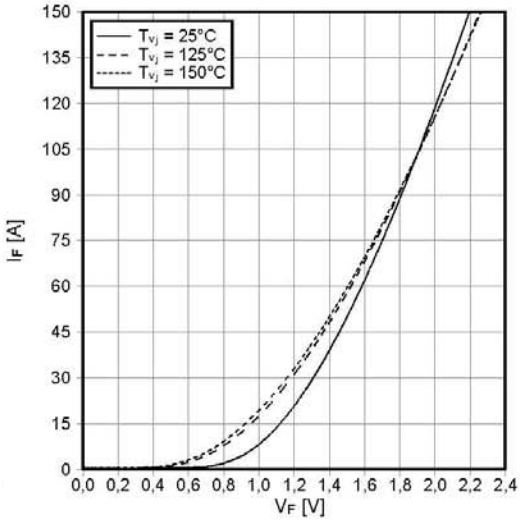
Transienter Wärmewiderstand IGBT-Wechselr.
transient thermal impedance IGBT-inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT-Wr. (RBSOA)
reverse bias safe operating area IGBT-inv. (RBSOA)
$I_C = f(V_{CE})$
$V_{GE} = \pm 15$ V, $R_{Goff} = 2.2\ \Omega$, $T_{vj} = 150°C$



Durchlasskennlinie der Diode-Wechselr. (typisch)
forward characteristic of diode-inverter (typical)
$I_F = f(V_F)$



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IGBT-Module
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Vorläufige Daten
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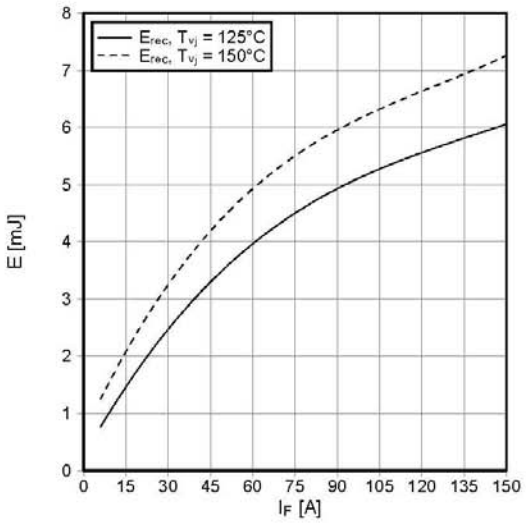
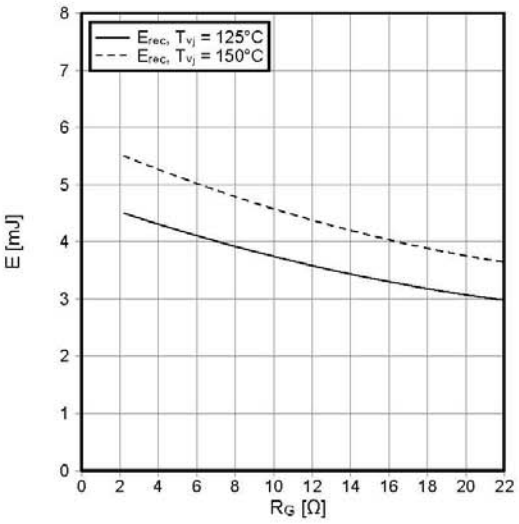
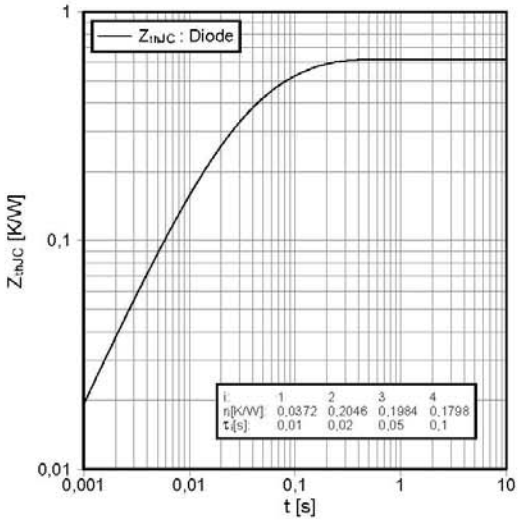
Schaltverluste Diode-Wechselr. (typisch)
switching losses diode-inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 2.2\ \Omega$, $V_{CE} = 600\ V$



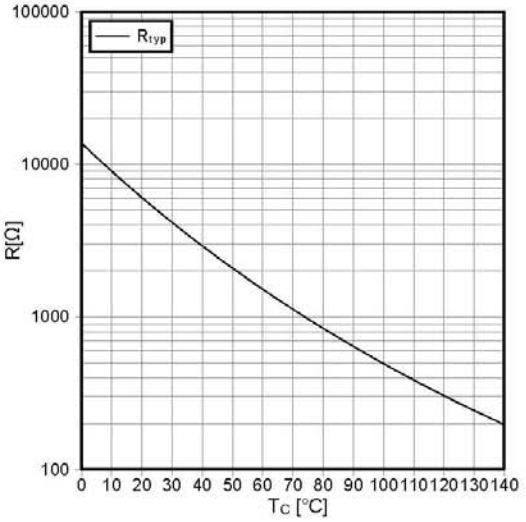
Schaltverluste Diode-Wechselr. (typisch)
switching losses diode-inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 75\ A$, $V_{CE} = 600\ V$



Transienter Wärmewiderstand Diode-Wechselr.
transient thermal impedance diode-inverter
$Z_{thJC} = f(t)$



NTC-Temperaturkennlinie (typisch)
NTC-temperature characteristic (typical)
$R = f(T)$



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Academic Profile

Jayalakshmi Kedarisetti

Born in East Godavari, India, on March 04th, 1982.

Since 2007	Working as an assistant at the Department of Power Electronics and Control of Drives, Technische Universität Darmstadt, Germany
2005 - 2006	Worked as a Project Associate in Power electronics group at Indian Institute of Science (IISc), Bangalore, India
2003 - 2005	Master of Technology in the area of Power and control in Electrical engineering at Indian Institute of Technology Kanpur (IITK), Kanpur, India
1999 - 2003	Bachelor of Technology in Electrical and electronics engineering at Jawaharlal Nehru Technological University, Kakinada, India